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Phil Noll, calibration lab manager at Hamilton Sundstrand.

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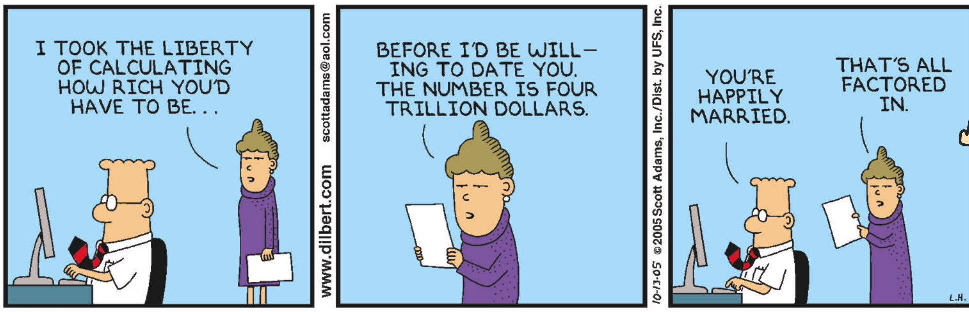

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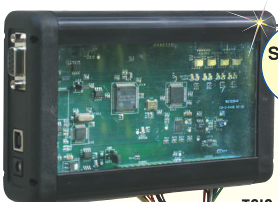

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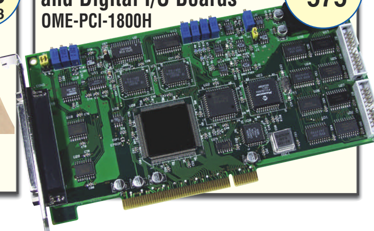

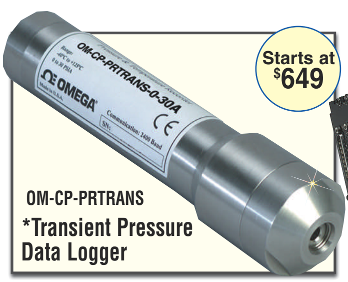

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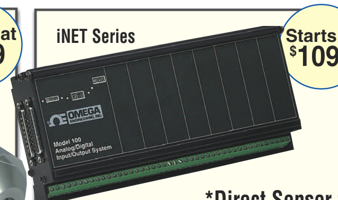

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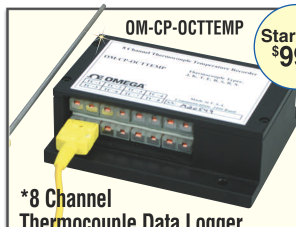

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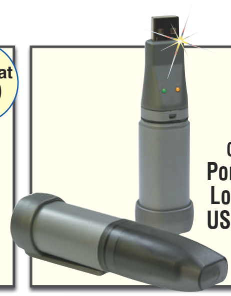

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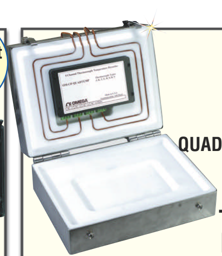

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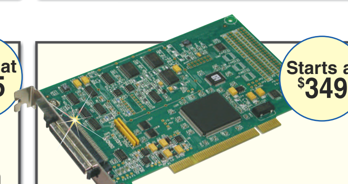

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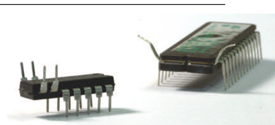

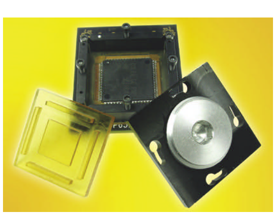

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Communications Test Report

- **Switching in the automated lab**
  Communications test labs often need to share test systems with remote locations. In this exclusive interview, Roberta Gonzalez, cofounder of EdenTree Technologies, discussed the role of switching systems in remote-access applications.

- **WiMedia test tools emerge**
  Certification standards for the WiMedia wireless networking radio are not yet finalized, but that has not deterred test-equipment developers, who are beginning to introduce products that support certification efforts.

- **Test metric tackles IPTV**
  IPTV poses challenges for engineers who must evaluate the performance of network equipment. The new Media Delivery Index metric provides insight into the Internet's ability to handle video.

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Automotive & Aerospace Test Report

- **Structural testing and calibration meet industry demands**
  Measurement data from the shop floor has become an indicator of part quality and process integrity. In this interview, Richard Bono, application specialist at The Modal Shop, shares his experience with techniques that improve manufacturing quality.

- **Test lab ensures compliance**
  Mark Abrahamson, an electromagnetic compliance engineer for vehicle testing at TÜV SÜD America, described his company's role in testing products for compliance with industry standards.

www.tmworld.com/aatr

Firms implement DFT for CDMA devices

When Qualcomm migrated to deep submicron processes, its engineers needed new test methods to handle delay defects at wafer sort and final test. In this Web-exclusive feature, Gaurav Bhargava and Michael Laisne of Qualcomm and Martin Amodeo of Cadence Design Systems describe an effort that successfully implemented DFT in multiple 90- and 65-nm designs.

www.tmworld.com/dft_cdma

Blog commentaries and links

"Taking the measure"

by Rick Nelson, Chief Editor

- Petaflop supercomputer on the way
- People are not dual-core processors
- Natural-language expert thwarts computer-language firms

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Stereotype threats

In our September cover story, we commented on the dearth of women in engineering ("Where are the women?" p. 32). Based on a recent study, one might assume women are simply not smart enough to excel in such a demanding field. John Philippe Rushton, professor of psychology at the University of Western Ontario, says he found that men are smarter than women (and not just in science and math) by 3.63 IQ points.

What prompts such research, and should it take place at all? It's difficult for someone trained in science and math to contend that some studies aren't worth doing. And I was uneasy with the uproar that forced Lawrence H. Summers to resign as president of Harvard after questioning whether innate differences between men and women might explain why fewer women succeed in science and math careers.

RICK NELSON, CHIEF EDITOR

But let's look further at the potential problems with studies like Rushton's that might address the questions like the one Summers put forward. First, we can't even define intelligence, let alone devise tools to accurately measure it. (See the online version of this article at www.tmworld.com/2006_10 for links to criticisms of Rushton's study.) But more pernicious is the damage that publication of the dubious results can cause.

It's difficult for someone trained in science to contend that some studies aren't worth doing.

As other studies have shown, a phenomenon called "stereotype threat" causes people prompted to think about negative stereotypes to conform to them. Specifically, women tend to perform poorly on math tests if you suggest to them before asking the questions that they might. But University of Texas psychologist Matthew S. McGlone has conducted a study showing evidence of a countervailing effect. When prompted to think about stereotypical strengths rather than weaknesses, people perform better.

In McGlone's study, he presented identical math tests to two groups of college students, each containing men and women. For one group, he prefaced the math test with questions about coed housing and other aspects of campus life that bring gender issues to the forefront. For the other group, he prefaced the math test with questions about how each student had come to be accepted at the elite liberal-arts college they were attending.

The result: Women subjected to the stereotype-threat questions about gender underperformed men by 25 to 30%. For the other group? "There was no significant difference between men and women," McGlone reported.

The so-called study Rushton performed and the question Summers posed amount to pervasive, culture-wide, and self-fulfilling stereotype threats that discourage women from trying to excel. T&MW

Post your comments at www.tmworld.com/blog.

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[An exclusive interview with a test engineer]

Keep the ink flowing

DAN GUIDERA

Richard Clark is a product engineer at Hewlett-Packard's Corvallis, OR, facility. He evaluates and characterizes ICs used in the print heads of inkjet printers. He performs most of his testing at the wafer level, controlled by drivers. In a recent interview, Clark described the measurements he performs using numerous test instruments. He also explained how he automates his tests and how he writes instrument drivers.

Q: What functions do the ICs perform?
A: The ICs are the electrical interface between the printer and the nozzles that eject the ink. They receive digital commands and control the firing of the ink nozzles.

Q: What measurements do you perform on an IC?
A: Starting with schematics and circuit descriptions as test guides, I evaluate the performance of analog components within the IC, including DACs, ADCs, current sources, amplifiers, voltage references, and resistances. The rack includes an LCR meter, a source-measure unit, an oscilloscope, and a VXI chassis that contains a DMM, a digital pattern generator, and a switch matrix. I use the pattern generator to simulate digital commands from the printer. The oscilloscope lets me check output waveforms that drive the print nozzles. I perform the analog and parametric tests with the LCR meter, DMM, and source-measure unit. The wafer under test sits atop a thermal wafer chuck.

Q: How do you automate your tests?
A: Because we use HP Unix workstations to control the instruments, I often have to write custom drivers in C for each instrument. Rather than use the drivers that come with instruments, I write drivers that perform specific measurements. A driver contains only the code needed to set up an instrument and make the measurements I need. Then, I use Vee version 4 to produce test sequences.

Q: How do you make use of the drivers?
A: The drivers let me change parameters such as voltage, frequency, or temperature before a series of measurements so I can produce plots of device performance. Once I import the driver into Vee, I can see the function and the input variable names. Often, that's enough information for me to understand what the function does. Source code comments provide additional information.

Q: How has automation improved the way you perform evaluations?
A: It doesn't pay to perform a manual test on a device. Because I have a library of test functions already written, I can run tests faster and easier using automation, particularly because each test may require repeated measurements using different parameters.

Q: What else have you done to streamline the tests?
A: I've developed interface boards that let anyone quickly connect instrument probes and cables to the wafer prober. The board becomes a "mini test head" that contains connectors, switches, and relays that minimize setup time.

Q: What do you do with the test results?
A: I share test results with designers so we can compare measured results against simulated results. Often, we find differences in how a device will work when integrated into a printer. A test is, in effect, an experiment.

Q: Why does a designer need to run tests?
A: Designers often place circuits on test wafers and then test the circuit using the automated test station. A designer can often find the driver's measurement functions he or she needs to run a test. If I can write a driver that someone else can use, I've improved productivity. T&MW

Every other month, we will publish an interview with an electronics engineer who has test, measurement, or inspection responsibilities. If you'd like to participate in a future column, contact Martin Rowe at mrowe@tmworld.com.

PCI, PXI modules and chassis support data acquisition

Adlink Technology America has released a series of cards and chassis addressing PXI and PCI data-acquisition applications. The company's $1195 14-bit DAQe-2010 and $1495 16-bit DAQe-2016 feature a maximum 2-Msamples/s and 800-ksamples/s sampling rate per channel, respectively, across a PCI Express x1 lane. The company also introduced standard PCI and PXI modules: the $1495 DAQ 2016 and the $1695 PXI 2016. Each provides 12-bit, 1-Msample/s performance. Each of the four new modules provides two 12-bit, 1-Msample/s analog outputs, two 16-bit counter/timers, and 24 channels of digital I/O. They include support for C/C++, Delphi, Visual Basic, .NET, Matlab, and LabView programming environments.

The new chassis introduced by the company include the $2600 14-slot compact PXIS-2670 (pictured), which measures 258x448.4x177.8 mm. A separate power partition accommodates 500-W power supplies by effectively dissipating heat and controlling radiated emissions. The company has also debuted two PCI chassis: the $1390 13-slot PCIS-8580-13S and the $1250 four-slot PCIS-8580-4S. Each of the PCI chassis makes use of a "serialized bridge" technique to support parallel PCI signal transmissions in four-pair, 622-Mbps serialized LVDS signals. www.adlinktech.com.

BP Microsystems changes name

BP Microsystems, a supplier of device programming systems, has announced that it will now be known as BPM Microsystems. The name change coincides with the opening of BPM Microsystems' new headquarters building in Houston, TX.

"Our new name will reflect the same high-quality company that customers and the industry alike have depended on for the past 21 years," said Lyman Brown, VP and COO. "However, we look forward to no longer being confused with BP Amoco, the oil company, who also has its headquarters in Houston."

The original BP name was created from the founders' first names—Bill White and Peter Cole—when they opened the company in 1985. BPM Microsystems continues today under the direction of CEO and president Bill White. www.bpmmicro.com.

Synopsys broadens DFM portfolio

Synopsys has announced that it has completed the acquisition of Sigma-C Software, a Munich-based company providing simulation software that allows semiconductor manufacturers and their suppliers to develop and optimize process sequences for optical lithography, e-beam lithography, and next-generation lithography (NGL) technologies. Synopsys acquired SIGMA-C in an all-cash transaction for $20.5 million.

The acquisition will enable Synopsys to more tightly integrate design and manufacturing tools, allowing customers

Editors' CHOICE

Scopes get bandwidth boost and analysis tool

LeCroy has increased the bandwidth of its four-channel WaveRunner Xi and WaveSurfer Xs oscilloscopes. The WaveRunner 204Xi now runs at 2 GHz, while the 104Xi runs at 1 GHz. The WaveSurfer 104Xs now runs at 1 GHz, an increase from 600 MHz.

All three scopes feature a new software tool for finding anomalies in captured waveforms. Called WaveScan, the software feature lets you specify any of 20 waveform parameters that differ from a "normal" parameter. Parameters include frequency, rise time, pulse width, greater than, less than, or inside or outside a range. The software also provides statistics on occurrences that meet your criteria. For example, you can get a distribution of edges that fail to meet a minimum rise time.

The three scopes also add decode and data trigger options for the I^2C and SPI data buses. CAN bus decoding was previously available.

LeCroy has also introduced two ZS Series 1-MΩ, 0.9-pF active probes with 1.5-GHz and 1-GHz bandwidths. The probes come with a kit of short leads that minimize inductance.

Prices: WaveRunner 204Xi—$22,250; WaveRunner 104Xi—$16,250; WaveSurfer 104Xs—$12,890. Probes: 1.5 GHz—$1190; 1 GHz—$490. *LeCroy, www.lecroy.com.*

to perform more accurate design layout analysis with 3-D lithography simulation and to understand yield issues for effective DFM implementation.

Sigma-C products complement Synopsys' design for manufacturing (DFM) and TCAD solutions, with SOLID+ providing analysis of variability within the lithography process on design layout in the DFM flow, and SOLID E providing lithography models for optimizing the lithography process. SOLID+ and SOLID E share a central database of lithography models to help ensure high accuracy and consistency of simulation results between design and manufacturing. www.synopsys.com.

Agilent completes acquisition of Xpedion

Agilent Technologies has announced it has completed the acquisition of Xpedion Design Systems, a privately held company that provides software for wireless and high-speed digital circuit and systems design in the communications industry. Financial details were not disclosed. By adding Xpedion's products to its portfolio, Agilent will increase its emphasis on design verification and design for manufacturing (DFM), giving customers a design flow covering RFIC design, design verification, and DFM. www.agilent.com.

CALENDAR

Vision 2006, November 7–9, Stuttgart, Germany. Sponsored by Messe Stuttgart. *www.vision-messe.de.*

Aerospace Testing Expo North America, November 14–16, Anaheim, CA. Organized by UKIP Media and Events. *www.aerospacetesting-expo.com/northamerica.*

Electronica, November 14–17, Munich, Germany. Sponsored by Global-Electronics.net. *www.global-electronics.net.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

Tidal enhances chamber controllers

Tidal Engineering has added a barcode/OCR reading feature to its multichannel, microprocessor-based Synergy controller. The environmental-chamber controller's new macro capability accepts digital data from a part's barcode/OCR label and implements the appropriate test profiles without further operator intervention.

The Synergy Controller uses the Microsoft Windows CE .NET embedded operating system and includes a front- or flush-mounted 320x240-pixel (color STN) touch screen. The controller assumes command of an environmental chamber's conditioning systems to facilitate the programming of temperature, humidity, altitude, and vibration versus time. In addition, operators can program up to six custom outputs. Temperature is measured using a 100-Ω platinum RTD probe or a thermocouple, whereas humidity is measured by an electronic sensor.

The controller's communications capabilities include RS-232, RS-485, Ethernet, and GPIB. Its Web-Touch Remote built-in Web server enables remote control and monitoring from any standard browser. A USB flash disk, 32 Mbytes of onboard flash, 32 Mbytes of SDRAM, and USB storage come standard.

Base price: $2750. A 30-day demo is free. *Tidal Engineering, www.tidaleng.com.*

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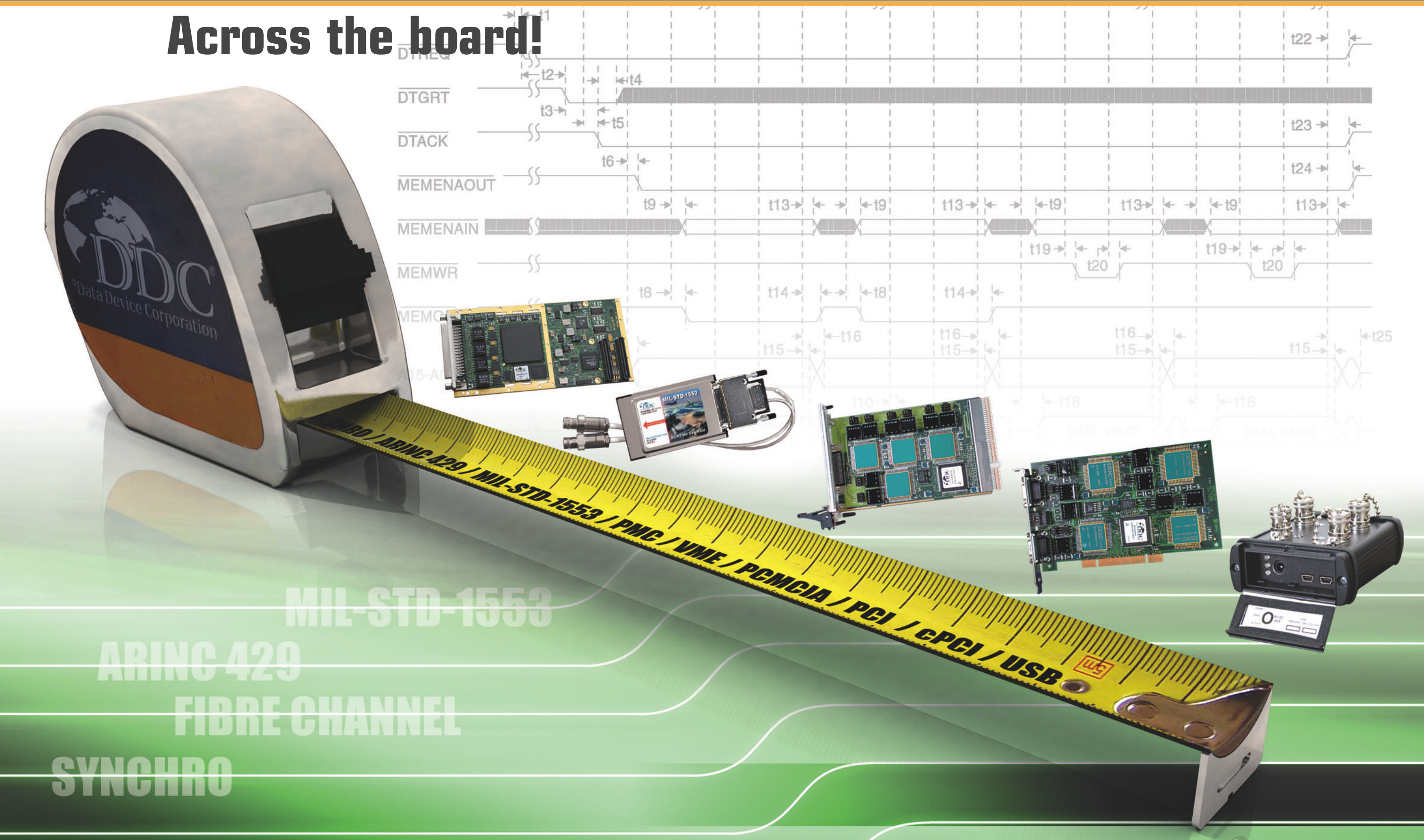

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EMC software takes center stage

> > > IEEE Symposium on Electromagnetic Compatibility, August 7–10, Portland, OR. www.emcs.org.

EMC design and test software was in abundance at this year's symposium. "EMC simulations are simply tests done with computers," said Bruce Archambeault, distinguished engineer at IBM. Software appeared from **IBM** (www.mossbayeda.com), **Ansoft** (www.ansoft.com), **Advanced Electromagnetics** (www.aemi-inc.com), **ScanCAD** (www.scancad.com), **Zeland Software** (www.zeland.com), **EMS-Plus** (www.ems-plus.com), **NEC** (www.emistream.com), **SimLab Software** (www.simlab-emc.com), and **Applied Simulation Technology** (www.apsimtech.com).

Software from **Flomerics** (www.flomerics.com) simulates PCB emissions. **Comsol** (www.comsol.com) also exhibited its general-purpose modeling software that includes electromagnetics. **Quantum Change** (www.quantumchange.com) offers software that automates EMC measurements in the lab, and **Traxstar Technologies** (www.traxstar.com) offers software for managing EMC labs.

Agilent Technologies (www.agilent.com) announced a return to the CISPR EMC compliance market when it previewed a CISPR-compliant preselector for frequencies up to 1 GHz. **Rohde & Schwarz** (www.rohde-schwarz.com) introduced a new FFT scan option for its EMI receivers that reduces measurement time. A management buyout of the Test Systems Division of **Schaffner** (www.schaffner.com) will result in a new company. The new company, which has not yet been named, will be headquartered in Luterbach, Switzerland; and Berlin, Germany.

TECHNICAL SESSIONS

This year, the technical sessions included papers that covered signal integrity. In one session, Antonio Ciccomancini of CST simulated the physical parameters of a 16-layer backplane over the 0–20 GHz range. In the "Extreme EMC" session, Ron Brewer discussed how today's spacecraft are tested to yesterday's EMC standards. Johan Catrysse gave a presentation about IEEE 1302, a standard that covers test methods for characterizing EMI shielding gaskets. Gang Feng of the University of Missouri-Rolla discussed a method for measuring EMI coupling paths in electronic systems. Robert Johnk explained how NIST worked with General Motors to characterize the company's automotive EMC test facility to provide uniform fields for immunity testing.

Brian Jones described how Britain is adjusting to the new EMC Directive, which becomes effective next year and receives full enforcement on 2009. Hirayr Kudyan discussed how he performs measurements on a system's power bus to predict the product's EMC performance before the product is completely designed. Ken Wyatt demonstrated the effects of ESD on electronic circuits. He creates ESD discharges to show how today's high-bandwidth oscilloscopes reveal more about ESD waveforms than was known when test standards were written. T&MW

For more details about the technical sessions and the products that were exhibited during the show, see our online reports from the EMC Symposium at www.tmworld.com/EMC_2006.

Ken Wyatt, EMC engineer at Agilent Technologies, demonstrated ESD waveforms on a high-bandwidth oscilloscope.

Voice and video continue to grow

> > > VON Fall 2006, Boston, MA, September 11–14, 2006. Pulver Media. www.von.com.

VON (which originally stood for Voice On the Net) has grown from a niche show into one that now boasts 250 exhibitors. Although voice over IP (VoIP), is still growing, video has really fueled VON's growth. The Fall 2006 edition of VON saw the emergence of IP Multimedia Subsystem Networks—a protocol that merges IP services with a range of access networks

Spirent Communications (www.spirentcom.com) introduced the Spirent Protocol Tester with predefined test cases for testing IP Multimedia Subsystem (IMS) core-network elements. As part of the announcement, Reef Point Systems demonstrated its security for voice and video calls that use IMS to provide network access. **Tektronix** (www.tektronix.com) announced Spectra2|VQM version 2.0 software for its Spectra2 network tester, which early IMS adopters can use in network test. Spectra2|VQM version 2.0 adds video-quality testing to its voice capabilities.

Radcom (www.radcom.com) announced Omni-Q for IPTV, an instrument that monitors IPTV networks for network quality (jitter and packet loss), video stream quality, video decoding, video stream statistics, and other parameters. **Ixia** (www.ixiacom.com) added capabilities to its Optixia modular test platform that support voice, video, and data testing. T&MW

To read about more products exhibited at VON and to learn about the panel sessions, see our online coverage at www.tmworld.com/VON_2006.

RICK NELSON
CHIEF EDITOR
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Challenges run gamut from timing to DFM

TEST ENGINEERS can expect to confront RF, memory, and compression-based-scan test challenges; perform timing measurements; deal with manufacturability and yield issues; and contend with soft errors. That observation is based on the line-up of new full-day tutorials planned for the International Test Conference, which will be held during the week of October 22 in Santa Clara, CA.

The ITC has added seven tutorials to the line-up it offered in 2005. Courtesy of the International Test Conference.

Six new advanced tutorials and one on test fundamentals will complement 10 updated sessions, bringing the roster to 17 total tutorials scheduled for Sunday and Monday, October 22 and 23.

ITC program committee member and ARM fellow Rob Aitken, who heads up the tutorial effort, said in a phone interview that the new tutorial on test fundamentals will meet the needs of 30% of attendees at ITC. Other tutorials will bring test veterans up to speed on emerging topics like RF design for test (DFT), for which a session will discuss how to extend techniques developed for mixed-signal test to the RF domain.

A tutorial on design for manufacturability (DFM) will demonstrate that DFM and yield issues are no longer the exclusive domain of designers. Said Aitken, "The final arbiter of yield is always test, so the interaction between them has to be understood." Yervant Zorian, chief scientist of Virage Logic, is one of the presenters of the DFM session, which will complement a DFM and yield workshop that Zorian has organized for October 26–27.

A tutorial on memory test might seem to cover old ground, but, said Aitken, what's new is that DFT engineers now must place test and repair circuitry on hundreds or thousands of memory blocks within 90-nm or 65-nm designs. "The purpose of the tutorial is to give a practical description of the issues involved and the tools available to help."

Other topics include digital timing measurement. "Test engineers are going to spend a lot of their time with oscilloscopes and other instruments trying to debug their devices and their tests," said Aitken. Another session will cover soft errors, which, he said, will occur not just in memories but in standard logic as well, as designs move toward 45 nm. Finally, a session on compression-based test will describe how to detect, analyze, locate, fix, and log failures based on compressed data.

Participation in the tutorials earns credits toward an IEEE Computer Society Test Technology Technical Council Test Technology Certificate.

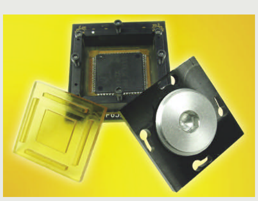
In addition to the tutorials, ITC will feature lectures—essentially mini tutorials—interspersed throughout the technical program. One called "Test Experiments and Case Studies" has this goal, according to Aitken: "By giving people the 'Science 101' about how to conduct a test experiment, we'll have more and better trained experimenters conducting more and better experiments and publishing their results at ITC. So, the whole community wins." T&MW

For a link to the transcript of my interview with Aitken, as well as a list of the seven new tutorials being offered at ITC, see the online version of this article. www.tmworld.com/2006_10.

Vimicro orders multiple J750s

Teradyne has announced that Beijing-based fabless semiconductor Vimicro International has selected the J750 as its major device test platform and has purchased multiple systems for testing multimedia processors. Dr. Edward Yang, director of chip operations and purchasing at Vimicro, said the selection was based on Teradyne's demonstrated level of customer support in China. www.teradyne.com; www.vimicro.com.

QFP socket exceeds 10 GHz



Ironwood Electronics' SG-QFE-7000 socket allows 0.4-mm-pitch, 14-mm-body QFP ICs to be used in socket in very-high-bandwidth applications. The 28-pin plus center-power-pad socket operates at 10 GHz with less than 1-dB attenuation. It can dissipate several watts without extra heat-sinking and can handle up to 100 W with a custom heat sink. The contact resistance is typically 23 mΩ per pin. Temperature range is –35°C to 85°C. www.ironwoodelectronics.com.

Verigy Q3 revenues up 81%

Verigy has reported revenue of $214 million for its third fiscal quarter ending July 31, 81% above last year. Orders were $199 million, up 36% over the same period a year ago. Third quarter net income on a GAAP basis was $13 million, taking into account $24 million of net charges related principally to Verigy's spin-off from Agilent Technologies. For the fiscal fourth quarter ending October 31, the company said it expects revenue to be from $185 to $200 million. www.verigy.com.

JON TITUS
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Protect your cameras

CAMERA demonstrations usually take place in clean or benign environments that come close to ideal. But cameras on production lines often must operate in toxic or dirty environments and must withstand shock and thermal stress. Cameras chosen for industrial use, therefore, require special protection—an aspect of system design engineers might forget.

Several years ago, in response to an auto manufacturer's requirement to protect cameras, Tectivity, a distributor of imaging components, developed a protective housing that accepts a variety of commercial cameras. "Our VideoModule protects a camera, as well as an optional LED light source, from heat, dirt, oil, physical damage, and tampering," said Jon Heywood, president of Tectivity. "A sealed hatch lets technicians quickly adjust lens settings without removing the camera and without disturbing the camera's calibration."

The protective enclosure that holds this camera gives technicians access to components and controls through hatches. Technicians can remove a front shroud and easily adjust a lens or filter. Note the use of chains and captive screws to keep parts nearby. Gaskets create a tight seal between the body and hatch lids. Courtesy of Tectivity.

Generally, it costs less than $500 to protect a camera, but costs increase when customers choose options such as internal light sources or special connectors. Most options and add-ons reside within a VideoModule enclosure. If a camera will point upward, at the bottom of a product, Tectivity can equip a VideoModule with an air blow-off and a mechanical eyelid that opens, lets a camera take a picture, and then closes to protect the camera.

Cohu Electronics offers cameras in sealed containers filled with dry nitrogen at a positive pressure of 5 psi. "You can hose down the enclosures without affecting the camera," explained Tim Jones, Cohu's OEM products manager. "We use a metal MIL-Spec connector on our enclosures, and we 'pot' the cable with a two-part epoxy to prevent the condensation of moisture, which could short-circuit signal pins." Cohu also offers a wash-wipe unit that can pump washer fluid to the camera and wipe grime off a transparent face plate.

In addition to being protected by special enclosures, cameras themselves must be able to withstand extreme temperatures. "Often, cameras must work at high temperatures and undergo many temperature changes, both of which can damage sensitive components," said Scott Massey, program manager at Dalsa. "We qualify our cameras to ensure they function properly across the 0°–50°C temperature span for their specified life."

To support operation in these extreme environments Dalsa offers cooling options, such as heat sinks or a capability to attach a solid-metal plate to a camera to dissipate heat. Cameras that operate under extreme conditions may require a special enclosure that should provide a way to cool a camera directly, noted Massey. Or, enclosures should include the means to attach passive or active cooling equipment.

Dalsa also tests cameras to ensure they stand up to jarring and rapid motion. "We test to guarantee the durability of the camera's electronics and to make certain the image sensor's alignment remains true," said Massey. "When a camera undergoes stress, its sensor must stay aligned." T&MW

MVTec offers vision kit

MVTec is offering the "Hands-on Machine Vision" kit to help its distribution partners demonstrate machine-vision functionality to prospective customers. The kit includes an aluminum case with sample industrial objects, illumination devices, and a camera, all of which can be combined with a notebook computer running the firm's Halcon software to form a complete machine-vision system. www.mvtec.com.

Cameras sport 1-GHz DSPs

Vision Components' VC44xx series cameras incorporate Texas Instruments' 1-GHz, 8000-MIPS DSPs and feature an RS-232 and an Ethernet interface as well as an external trigger input. Standard features also include a high-speed encoder interface. The first camera in the series, the VC4466, has a ⅓-in. CCD sensor with a 1024x768-pixel resolution and a maximum frame rate of 30 frames/s (60 frames/s in binning mode). www.vision-components.com.

Credit-card-sized camera weighs 21 g

Basler Vision Components is offering a board-level version of its A600f camera. The CMOS-sensor based camera has a full-frame shutter that can operate at 100 frames/s at 656x491-pixel resolution. The camera includes an IEEE 1394 interface and an area of interest (AOI) feature that allows it to operate with higher frame rates at lower resolutions. www.basler-vc.com.

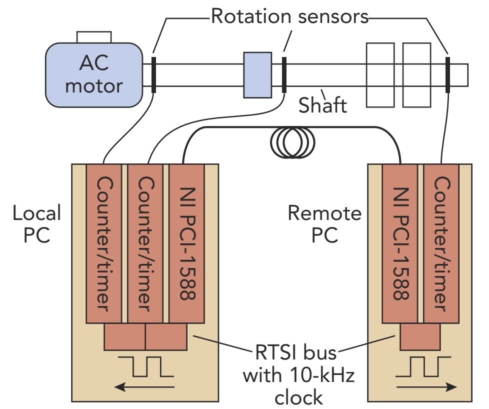
INSTRUMENTS

IEEE 1588 supports distributed test systems

Engineers often develop centralized measurement systems when they need precise timing across dozens or even hundreds of channels. When used in large applications such as aircraft wing measurements, centralized systems need long wires. Of course, long wires are likely to pick up interference, which reduces measurement accuracy. Decentralized, or distributed, systems can use shorter wires but can suffer from synchronization errors.

You can improve the timing of decentralized systems by taking advantage of IEEE 1588, "A Precision Clock Synchronization Protocol for Networked Measurement and Control Systems," which lets you synchronize measurements to less than 1 µs. That capability is what prompted the LXI Consortium (www.lxistandard.org) to choose IEEE 1588 as part of its instrument standard. With such precise synchronization, you can build a reliable distributed measurement system where you might otherwise need a centralized system.

To compare centralized and distributed systems, Alex B. McCarthy, senior product marketing manager at National Instruments, conducted an experiment using a rotating shaft. McCarthy used three shaft encoders that produced 2500 ticks/revolution to measure shaft rotation. The centralized system used one PC that contained three counter cards to count encoder pulses. The distributed system used two PCs, one with one counter card and the other with two. Each PC in the distributed system contained an IEEE 1588 interface card. At 2160 rpm, the encoder's tick period was 11.1 µs. Synchronization error in the distributed system was just 230 ns, which was insignificant in this application.



Two computers use IEEE 1588 interface cards to synchronize their measurements.

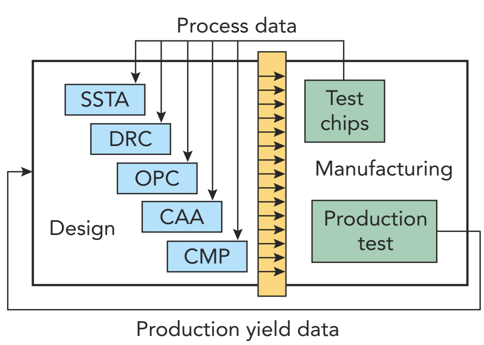
To learn more about McCarthy's application, you can download a zip file that contains his paper, "LXI uses IEEE 1588 PTP to Simplify Large-Scale Measurement Systems," from the online version of this article at www.tmworld.com/2006_10. The zip file contains LabView code used in the IEEE 1588 example as well as links to related articles about IEEE 1588.

Martin Rowe, Senior Technical Editor

DESIGN FOR MANUFACTURE

DFM, DFY get EDA industry emphasis

Design for manufacturing (DFM) and design for yield (DFY) are becoming increasingly hot topics as EDA companies attempt to help chip makers contend with random defects and process variations that can prevent fast, profitable ramp to volume in 65-nm and below process technologies. Tools addressing DFM and DFY issues are available from the big EDA firms, including Cadence, Magma Design Automation, Synopsys, and Mentor Graphics. Such tools provide optical proximity correction (OPC) and support resolution (or reticle) enhancement technology (RET), they provide critical area analysis (CAA) and address the effects of chemical mechanical polishing (CMP), they enable manufacturing-aware design rule checking (DRC), and they can perform parametric yield measurement and optimization. Beyond those functions, Cadence's Precision Router lets designers model manufacturing effects during the design process.



DFM and DFY tools overcome the one-way barrier between design and production; they make use of or assist in the capture of manufacturing data for use in the design process.

The big firms tout the smooth melding of DFM/DFY tools with other design-flow components. "Only an integrated solution closes the DFM gap to address yield issues," said Anantha Sethuraman, Synopsys VP for DFM.

John Lee, GM of the physical verification business unit at Magma Design Automation, noted that integration extends to foundries' reference flows, pointing out as an example that Magma tools have been qualified by IC-manufacturer TSMC.

Conversely, point-tool makers emphasize a laser-like focus on a particular DFM/DFY niche: "Our motivation in starting Stratosphere Solutions was to build differentiated technology that meets a focused market demand," said Prashant Maniar, chief

DFM, DFY get EDA industry emphasis *(continued)*

strategy officer of the firm, which develops silicon intellectual property (IP) designed to help silicon manufacturers reach DFM and DFY goals through process-variability characterization.

What DFM and DFY tools generally have in common is the ability to make use of actual manufacturing data in the design process or to assist in the capture of such data. OPC, CMP, and CAA tools generally work with test-chip data, which can be captured with the aid of Stratosphere's StratoPro, for example. Tools like Mentor Graphics' YieldAssist moves beyond the test-chip level to continually obtain yield-enhancement data from production-test systems.

Some DFM/DFY tools don't attempt to alter a design to comply with manufacturing requirements—they just give you a more accurate picture of how your design will translate to real silicon. Steve Smith, senior director of marketing for the Synopsys Galaxy platform, cited an example: For one chip, a worst-case-corner analysis indicated a customer could guarantee only 404-MHz performance, whereas the Synopsys PrimeTime VX variation-aware statistical static timing analyzer (SSTA) showed a 99% probability that the chip would run at 474 MHz.

See the online version of this article at www.tmworld.com/2006_10 for links to detailed information on DFM/ DFY tools and suppliers.

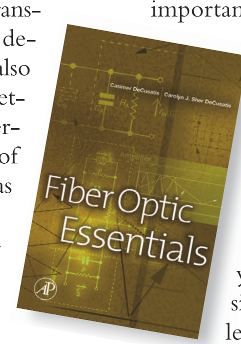
Rick Nelson, Chief Editor

BOOK REVIEW

A quick course in fiber optics

Fiber Optic Essentials, Casimer DeCusatis and Carolyn J. Sher DeCusatis, Academic Press (books.elsevier.com), 2006. 271 pages. $49.95.

Fiber Optic Essentials lives up to its name. In fewer than 300 pages, you will learn about the fundamentals of fiber optics, from the fiber itself to the transmitters and receivers to the design of FO systems. You'll also get a brief exposure to network protocols and to fiber-optic applications outside of communications, such as medical imaging.



The authors pack a tremendous amount of information into the first three chapters without overwhelming you. By the time you finish chapter 1, you'll have a grasp of how light travels through fibers and why connectors and proper alignment are important. You'll also learn about waveguides, single-mode fiber, multi-mode fiber, and plastic fiber.

After reading chapters 2 and 3, you'll have an understanding of transmitters and receivers. You'll learn how LED and laser light sources illuminate fibers and which specifications are important. On the receiver side, the authors cover how PN and PIN photodiodes convert optical pulses into electrical signals. By chapter 4, you'll be ready to put a fiber-optic link together. You'll learn how to develop a loss budget and how the all-important signal-to-noise ratio (SNR) and bit-error rate (BER) parameters affect a link's health.

After spending a chapter covering repeaters and optical amplifiers that lengthen links, the authors explain how wavelength multiplexing lets you send multiple transmissions through a fiber. You'll also learn about test equipment that can produce eye diagrams and calculate BER. Finally, you'll get an overview of optical-communication protocols. The book wraps up with a glossary and a list of acronyms.

My only minor criticism is that during their discussion of BER in chapter 3, the authors should have mentioned that the book has a further discussion of BER in chapter 8. Other than that, I found this book useful and educational. (Disclosure: The book's publisher is owned by *Test & Measurement World*'s parent company.)

Martin Rowe, Senior Technical Editor

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FIBER-OPTICS TEST

Vehicle buses get the light

DEVICE UNDER TEST

Automotive-grade and consumer-grade plastic fiber-optic transceivers designed for automotive optical serial buses such as Intelligent Transportation System Data Bus-1394 (IBD-1394) and Media Oriented Systems Transport (MOST). The devices send and receive light over plastic optical fiber at data rates up to 250 Mbps. Their primary use is for carrying digitized audio and video.

THE CHALLENGE

Test the transceivers during production for parameters such as average optical output power and current consumption. On the receiver side, measure output voltage levels and pulse timing.

THE TOOLS

- Agilent Technologies: bit-error-rate tester, high-speed oscilloscope. www.tm.agilent.com.
- Keithley Instruments: source-measure unit. www.keithley.com.
- National Instruments: graphical programming language. www.ni.com.
- Newport: optical power meter. www.newport.com.
- Singlewell Industrial: test handler. www.singlewell.com.tw
- Stanford Research Systems: clock generator. www.thinksrs.com.
- Tektronix: oscilloscope. www.tektronix.com.

PROJECT DESCRIPTION

Firecomms (Cork, Ireland, www.firecomms.com) manufactures fiber-optic transceivers used in IBD-1394 and MOST automotive optical serial buses. Each transceiver consists of a resonant-cavity LED (RCLED) and an LED driver IC for transmitting data. The device's receiver section consists of a pin diode and a combination transimpedance amplifier and limiting amplifier. The IBD-1394 transceivers use low-voltage differential signaling (LVDS), while the MOST devices use TTL-level electrical signals.

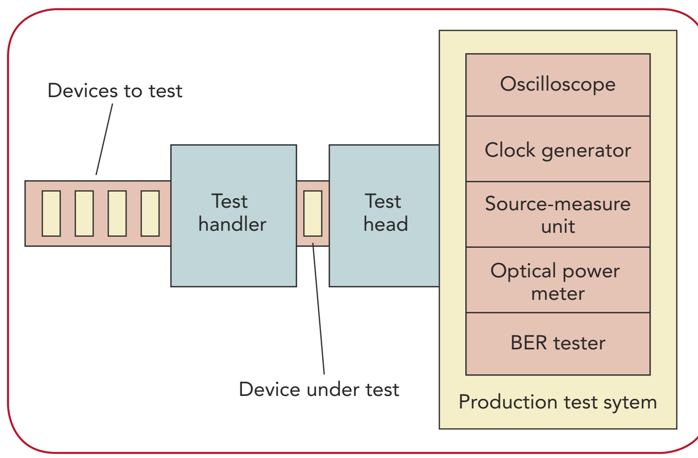
A production test system performs functional checks on all devices. The completed parts arrive at a device handler in tubes that hold about 50 devices. The handler moves the DUT to a test head that makes connections to test equipment.

To perform an average-optical-power test on a transmitter, a clock generator produces a clock signal that excites the transmitter at the device's maximum bit rate. An optical splitter divides the DUT's optical output, with 50% going to a plastic fiber that connects to an optical power meter. The system measures average optical power over a –40°C to 95°C temperature range for a known input current. The remaining optical power goes to a 650-nm optical detector that connects to an oscilloscope, which measures the rise time, fall time, pulse width, and pulse amplitude of the optical pulse.

Production tests also include measurements on the receiver circuits. Here, a "golden" Firecomms RCLED transmitter sends a calibrated light level through a plastic fiber to the DUT. A bit-error rate (BER) tester generates a PRBS7 data pattern for the RCLED to send to a receiver under test to simulate bus traffic. An oscilloscope measures the differential output voltage swing and timing parameters of the receiver's electrical output.

The transceivers have a so-called "wake-on-LAN" feature. When not in use, the device enters sleep mode to conserve power, returning to full power when it receives data. The test system's source-measure unit measures "sleep current" drawn through the DUT's power pins. Maximum allowable sleep current is 10 µA.

Firecomms also makes consumer-grade IEEE 1394 optical transceivers that receive the same tests as their automotive cousins, but over a smaller temperature range: –20°C to 70°C. For commercial-grade components, Firecomms tests transmitters with a 40-MHz clock instead of the 250-MHz clock used in automotive-grade devices. "A 40-MHz clock is fast enough to give us a high degree of confidence in the part," said CTO John Lambkin.



A production test system measures optical power, differential voltage swing, and timing.

LESSONS LEARNED

"Signal integrity is important in testing these devices," commented senior engineer Mike O'Gorman. "Sending 250 Mbps through cables and test pins to probe a part requires careful design. It has to be correct every time because of the hostile production environment with vacuum pumps running on the next bench, and molding presses hammering out parts close by." O'Gorman uses high-quality cables and BNC and SMA connectors to maintain signal quality. "Don't skimp on the cables" he advised.

Martin Rowe, Senior Technical Editor.

Engineers at Hamilton Sundstrand keep astronauts comfortable by calibrating systems that test environmental controls in spacecraft and space suits.

CALIBRATING SPACE

MARTIN ROWE, SENIOR TECHNICAL EDITOR

Phil Noll, calibration lab manager at Hamilton Sundstrand, stands among the mannequins in the company's space-suit museum.

FJ GAYLOR

WINDSOR LOCKS, CT—Space is one hostile environment. There's no air to breathe nor gravity to hold you down. Temperatures are frigid where the sun doesn't shine and burning hot where it does. Anything that generates heat has no air to cool it. Thus, equipment and astronauts would overheat without proper cooling.

Companies who design and manufacture equipment destined for space must carefully calibrate their products to withstand the hostile conditions, and they must subject the products to rigorous test regimens before delivering them. One such company is Hamilton Sundstrand Space, Land, and Sea Systems-Windsor Locks (SLS-WL), which has been making space suits since the 1970s. The company also makes environmental controls for the Space Shuttle and the International Space Station as well as for aircraft and submarines.

Environmental controls in space must perform perfectly under extreme conditions; there's no way to recall a product from orbit without great expense. Pumps, tanks, heat exchangers, motors, sublimators, evaporators, regulators, and electronics that control environmental systems need extensive testing before they launch. The systems that test these components must simulate conditions in space. The equipment that makes performance measurements and monitors the environment must be accurate—and that means regular calibration.

Simulating space and testing environmental systems requires SLS-WL to make many physical measurements, all of which require calibrated equipment. Instrumentation in test stations, called "test rigs," measures temperature, pressure, liquid and gas flow, vacuum, humidity, dew point, and vibration. Some of the company's test rigs date back to the Apollo program—SLS-WL provided the original lunar space suit—but they've been refurbished to meet current needs.

Table 1. Electronic calibrations performed in SLS-WL metrology lab

FUNCTION	RANGE	UNCERTAINTY
Voltage	1100 VDC	7 ppm @ 10 VDC
Voltage	750 VAC	80 ppm @ 10 VAC
Current	20-ADC source	90 ppm @ 1 A
Current	300-ADC measurement	0.04%
Power	6000-W AC/DC	0.02% full scale
Power	Power factor	90° lead / lag
Resistance	100 MΩ	12 ppm @ 10 kΩ
Frequency	10 µHz through 225 MHz	0.06 ppm
Time		± 0.06 ppm

Electronic test equipment used throughout the SLS-WL facility measures voltage, current, resistance, time, frequency, power, and phase. The test rigs employ data-acquisition systems that record physical measurements from transducers such as temperature probes, pressure gauges, and flow meters.

As you might expect, the Hamilton Sundstrand facility is loaded with environmental chambers. Temperature chambers, for example, test products over the wide range of temperatures encountered in space, with temperature cycling from –100°F to 350°F. Temperature/humidity chambers test at –100°F to 250°F at 10% to 98% RH. Thermal vacuum chambers test products down to 10^{-8} Torr and over temperatures from –300°F to 300°F.

Cool water

The Hamilton Sundstrand space suits, or Extravehicular Mobility Units (EMUs), have environmental systems that include oxygen and water tanks, batteries, a sublimator, fans, and regulators. These systems reside in a backpack with astronaut controls accessible through a front display and control module (**Figure 1**).

Pressure testers ensure that the tanks and tubes on the EMUs won't fail. For

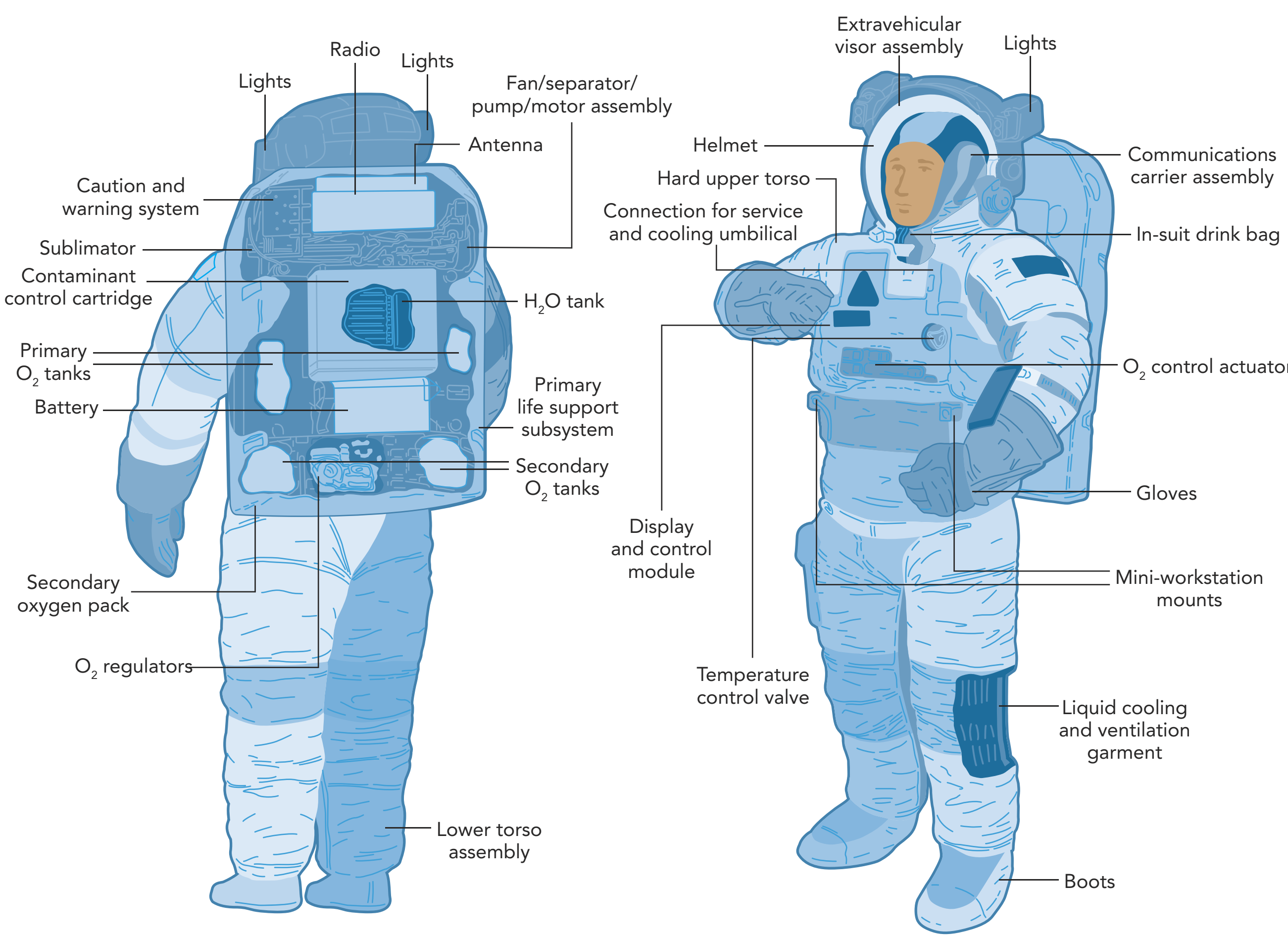


FIGURE 1. A space suit, called an Extravehicular Mobility Unit (EMU), contains oxygen tanks, cooling systems, and other environmental controls that require rigorous testing. Courtesy of Hamilton Sundstrand.

example, an oxygen tank, which operates at approximately 7600 psig, is tested with supply pressures up to 10,000 psig. (The high tank pressure is necessary to supply enough oxygen for a spacewalk while keeping the tank sufficiently small.) Vacuum leakage testers verify that parts don't leak water or oxygen into space.

Water in a space suit? Yes, and it's not for drinking (although the EMUs do have an in-suit drink bag). "An astronaut on a space walk has a high metabolic rate," said calibration lab manager Phil Noll. To keep astronauts cool, space suits are water cooled. They need a water tank, tubes, a pump, and a sublimator to extract the heat from the water.

Engineer for methods and standards Scott Shepard (back) develops calibration procedures and provides technical assistance to the metrology lab. Technician Dave Zisk (foreground) calibrates and certifies instrumentation used for production testing of environmental controls.

FJ GAYLOR

The SLS-WL Thermal Vacuum Space Simulator includes a data-acquisition system that technicians use to make measurements from specifications written by test engineers. Several Hewlett-Packard 3852A data-acquisition systems have been in place since the late 1980s. As long as these instruments are calibrated, they continue to provide valid measurements.

"We're not very quick to change instruments, because our test sheets are written to specific requirements and all equipment has been safety certified for each application," said Noll. Because many of the products produced in Windsor Locks remain in production for years, so do their test rigs.

Not all data-acquisition systems date to the 1980s. For example, a thermal chamber that tests Flight Releasable Attachment Mechanism (FRAM) systems con-

Into the earth

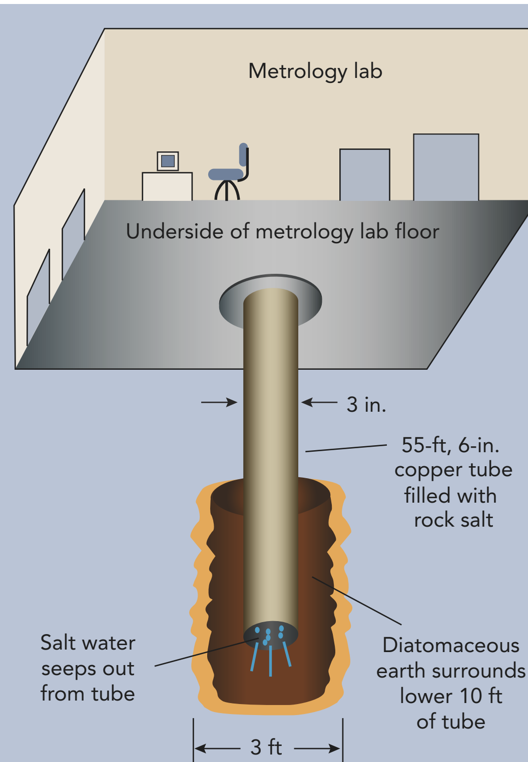
Engineers and technicians in the SLS-WL metrology lab must make measurements as accurately as possible. A key component of minimizing measurement uncertainty is stability, both in the environment and in the way instruments and systems are grounded.

Environmental controls maintain the lab's temperature and humidity. Engineers monitor those conditions 24 hours a day. Temperature and humidity dataloggers connect to a networked PC, which provides data through the lab's intranet Web page.

Maintaining a stable electrical ground is also crucial in achieving consistent measurements. Thus, the lab has a specially designed grounding system. The **figure** shows a 55-ft, 6-in. copper tube with holes at the bottom embedded into the ground. Diatomaceous earth surrounds the lowest 10 ft of the tube.

Because the earth at the bottom of the tube is cooler than that at the top (the lab floor), the tube draws heat from the lab. As the air cools, it creates condensation, which provides a solid bridging, self-maintaining ground system. Specific electrical outlets in the laboratory are connected to this ground plane. Appropriate fuses ensure safe operation at all times.

Martin Rowe, Senior Technical Editor



The metrology lab's grounding system consists of a copper tube embedded into diatomaceous earth under the floor.

nects to relatively new measurement equipment: data-acquisition cards installed in an industrial PC that runs National Instruments' LabView.

Used on the International Space Station (ISS), FRAM systems consist of a passive FRAM and an active FRAM, and they let astronauts transport cargo between the Shuttle Orbiter and the ISS. One passive FRAM is permanently mounted in the Orbiter's cargo bay, and another is mounted on the ISS. An active FRAM containing cargo is mated to the passive FRAM in the Orbiter. Should equipment in the ISS need replacement, astronauts can transfer the active FRAM from the passive FRAM on the Orbiter to the passive FRAM on the ISS.

A FRAM thermal/vacuum test subjects the mechanism to temperatures from –140°F to 260°F with vacuum well below 10^{-4} Torr. The FRAM system is mounted on a test stand where custom motors move FRAM mechanisms into place. Technicians use transducers and a data-acquisition system to measure torque (in. lbs) and force (lbs) while also measuring temperature and vacuum.

The FRAM test rig is one of several that requires calibration of its test instruments right at the rig. "We calibrate each parameter end to end in place," said Noll. A technician rolls an equipment cart containing the required stimulus to the rig in order to perform the calibration.

Table 2. Calibration labels and their meanings

COLOR	STATUS
Green	Item is within acceptable tolerance and is ready to return to its test rig
White	Item is within tolerance but not issued to a test rig (put on the shelf)
Yellow	Item is calibrated over a limited range

Safety precautions

Some tests require special test areas because of safety issues. For example, the company has an area outside the main building where technicians assemble the pumps and equipment that provide the high-pressure oxygen and nitrogen necessary for EMU testing. This test lab contains intrinsically safe and explosion-proof systems.

To test the EMU's high-pressure O_2 tanks, technicians start with liquid oxygen or nitrogen, change it to a gas, and initially pump the tanks to approximately 2200 psig. While monitoring air quality and pressure with a data-acquisition system, they increase the pressure to 10,000 psig.

During testing of the O_2 tanks, an HP 3852A data-acquisition system collects temperature, pressure, and flow data and

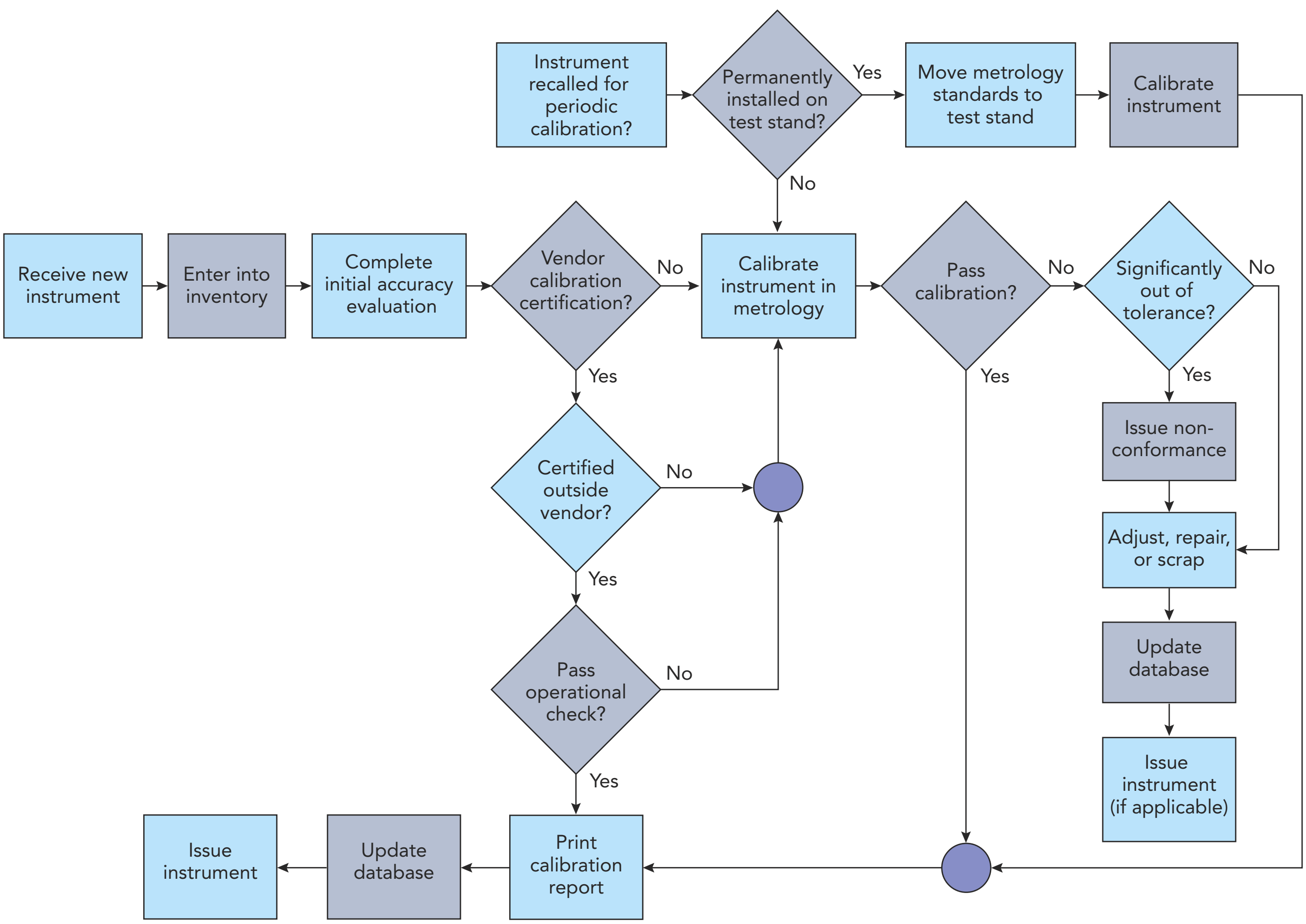


FIGURE 2. Permanently installed measurement equipment receives calibration while installed in a test rig. All other equipment is calibrated in the metrology lab. Courtesy of Hamilton Sundstrand.

Technician Dave Bates certifies all calibration standards used in the Hamilton Sundstrand SLS-WL metrology lab.

FJ GAYLOR

sends the data to a computer at the operator's console. The console contains two monitors, one for the operator and another for a test engineer. While the technician runs the test and monitors the performance of the test rig, the engineer monitors the item under test, keeping track of parameters such as coolant flow, pressure, and temperature.

The measurements that these test rigs perform start with a specification. A design engineer who needs a measurement provides the requirement to metrology engineering. Metrology engineers write a measurement specification that contains information such as measurement type, range, scale, and accuracy. Often, an existing test rig has the measurement capability that the design engineer requires. A test technician and metrology engineer review the measurement specification and decide which existing test rig to use or, if necessary, what the requirements are for new equipment.

The calibration lab

Sensors, meters, and other equipment used on test rigs as well as the test equipment used in manufacturing and engineering need calibration. That's the job of engineers and technicians in the metrology lab. The lab consists of several calibration stations as well as a station for documenting and labeling equipment. (For a discussion of the metrology lab's construction and grounding system, see "Into the earth," p. 30. The online version of this article contains a floor plan of the metrology lab.)

The electronic calibration station consists of two identical racks. Each contains a Fluke 5700 multifunction calibrator, an Agilent 3458A digital multimeter (DMM), and a Yokogawa power analyzer. In addition, the engineers can add instruments that provide any other required electrical stimulus. The stations calibrate DMMs, oscilloscopes, counters, power meters, data-acquisition systems, and other equipment that needs electrical input or measurement—about 1500 instruments. "We calibrate all the instruments used in SLS-WL," said Noll. **Table 1** shows the capabilities of the electronic calibration stations.

The lab also houses calibration references. Under the care of senior electrical technician Dave Bates, standards such as the Fluke 732B voltage references remain powered at all times, which maintains their stability. Bates uses these references to check the multifunction calibrators. Every two years, the calibrators, system DMMs, and voltage reference return to their respective manufacturers for calibration.

At the time of my visit, technicians still performed manual calibrations on electronic instruments. To automate the calibration procedures, SLS-WL metrol-

ogists are implementing Fluke's MET/CAL software. Although MET/CAL has many automated calibration procedures that cover much of the SLS-WL test equipment, most procedures need to be modified to meet specific lab needs.

Vibration is an important test for space-bound equipment, and the metrology lab has a dedicated accelerometer calibration station. At the time of my visit, the accelerometer calibration station—a rack of equipment—was about to be replaced by a benchtop instrument manufactured by PCB Piezotronics. The existing Bruel & Kjaer system had been in use since the 1980s and has a frequency range of 5 Hz to 10 kHz. The new system has a wider frequency range: 3 Hz to 50 kHz.

"Calibrating accelerometers requires a certain amount of finesse" said Noll. He pointed to the way an accelerometer under test was placed in the calibrator's test fixture. The sensor's wires must be held down so they don't vibrate relative to the sensor.

Temperature calibration

Across the lab from the electronic and accelerometer calibration stations is the temperature-calibration area. Here, technician Dave Zisk calibrates temperature probes used throughout SLS-WL. He calibrates some probes in the metrology lab, but probes installed in test rigs must be recertified in place.

In the lab, Zisk has several options for calibration. An oven that contains a 25-Ω standard platinum resistance temperature detector (SPRTD) probe lets him compare a probe under test to a known calibrated probe. He also uses thermal wells and oil baths to calibrate "working" probes—those used in the facility's test labs. The box on this page highlights the metrology lab's temperature-calibration capabilities.

An instrumentation rack connected to the SPRTD and probe under test contains an HP 3456 DMM, which measures four-wire resistance from RTD and thermistor probes and measures voltage from thermocouple probes. A reference junction provides a 32°F reference for the instrumentation, and a switch system connects the probes and reference junction to the DMM. A PC running LabView stores resistance measurements from the SPRTD and probe under test. The software includes the calibration curve for the SPRTD and also converts the resistance measurements to temperature. Then, software generates a calibration curve for the probe under test from resistance or voltage measurements.

To calibrate probes installed in the test rigs, Zisk uses a "Black Stack" thermometer from Hart Scientific. The thermometer measures temperature from a standard probe under test, from which a laptop computer calculates the probe's new resistance-temperature curve.

SLS-WL has six standard platinum probes. Technicians use five to calibrate working test devices. A sixth remains in the metrology lab as a check for the other five. These standard probes require calibration, too. Because they are the facility's reference probes, they need to be

Temperature-calibration capabilities

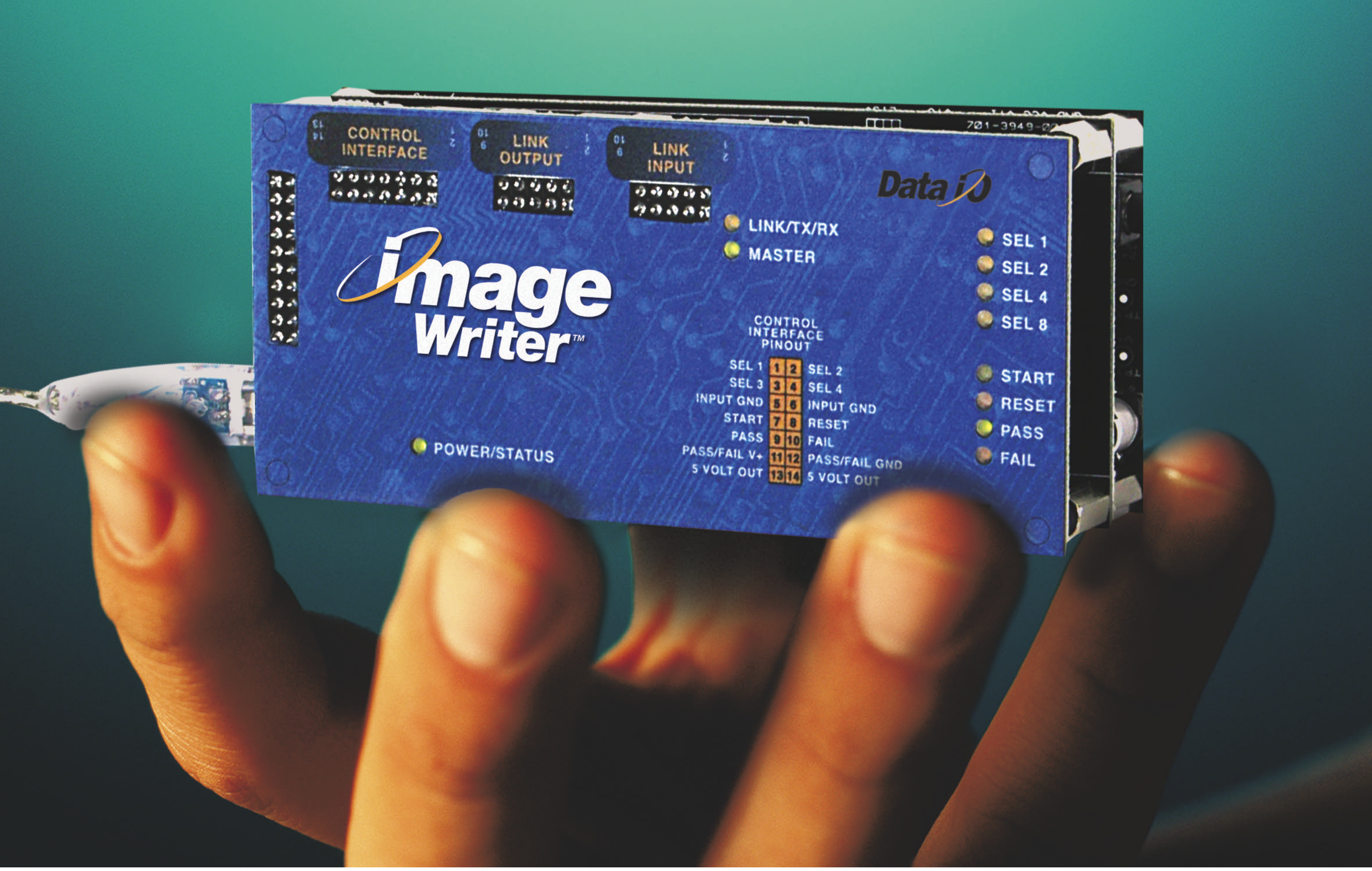
Automatic calibration system: Rig 257

Automatic or manual calibration of
- thermocouples
- RTDs
- thermistors
- temperature switches
- thermometers

Technology:
- oil bath vs. SPRTD
- thermal well vs. SPRTD
- thermal well vs. standard thermocouple
- oven vs. SPRTD
- aluminum freeze point (1220.5814°F)
- zinc freeze point (787.24°F)
- tin freeze point (449.55°F)
- gallium melt point (85.57628°F)
- water triple point (32.018°F)
- mercury triple point (–37.90192°F)

Range: –65°F through 2000°F

Uncertainty: SPRTD: 0.036°F



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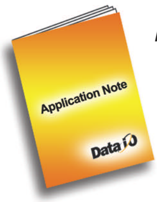

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calibrated at known, stable, and repeatable temperatures.

The metrology lab contains several Isotech fixed-point temperature cells that serve as primary temperature standards. The cells contain mercury, gallium, zinc, tin, aluminum, and water from which they achieve freezing points or melting points of these elements as well as the triple point of water (Ref. 1). Metrologists maintain a gallium cell—melting point 85.57628°F—at all times that they use as a quick check for damage to any of the six standard probes

"We use the primary standards at six-month intervals," said Noll. When I asked how Hamilton Sundstrand can justify the cost of these primary standards, Noll replied that an SPRTD calibration can cost up to several thousand dollars, and the company comes out ahead in the long run by purchasing its own primary standards and by being able to obtain immediate verification of standards accuracy.

Data collection and tracking

Accurate and complete calibration data is essential for a company to prove that its test equipment is operating within acceptable parameters. Several SLS-WL customers and accreditation agencies audit calibration procedures and records regularly. On the day of my visit, Scott Shepard, engineer, methods and standards, was working with a NASA audit team. The SLS-WL "Gage Recall System" ensures compliance with MIL-STD-45662A, ANSI Z540, AS 9100, ISO 9000, and ISO 17025. The system includes a relational database and an intranet Web page.

For each item that requires calibration, the database stores information such as calibration results, calibration dates, the next recall date, and the location of each instrument and accessory used for electrical, mechanical, or physical measurements during the calibration. Every item that requires calibration has a serial number and bar code for easy tracking.

Because the database tracks hardware test information, engineers always know which products were tested with each gage. The system displays data on the lab's intranet, where technicians and engineers can view the calibration information.

Figure 2 shows the flow of an item as it passes through calibration. The figure highlights two paths, depending on whether the item is to be calibrated at SLS-WL or at an outside calibration house. Following calibration, a technician places a green, white, or yellow label on the item before returning it to its location or placing it on the shelf. All items that fail calibration receive a red sticker. **Table 2** shows the label colors and what they designate.

Hamilton Sundstrand's Space, Land, and Sea metrology lab supports instrumentation used for numerous electronic, physical, and dimensional measurements. Calibration of measurement equipment used in test rigs ensures that the company's environmental controls will keep astronauts safe and comfortable in space. T&MW

REFERENCES

1. For information on the freezing, melting, and triple points of various substances, see the International Temperature Scale of 1990 (ITS-90), Table 1. www.its-90.com/table1.html.

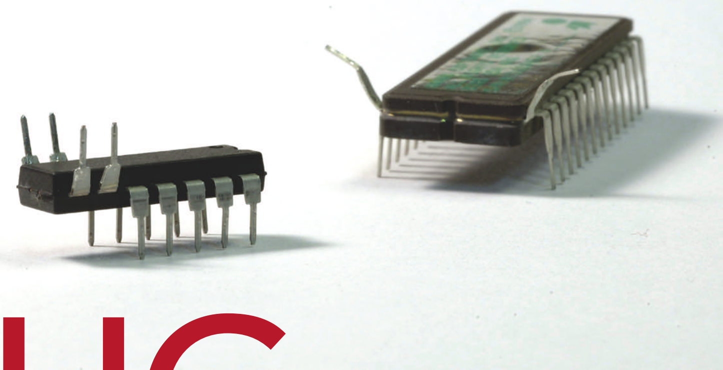
ON THE WEB

The online version of this article includes a floor plan of Hamilton Sundstrand's metrology lab. **www.tmworld.com/2006_09**

Interested in learning more about testing equipment for space? Check out these articles by Martin Rowe that appeared in previous issues of *T&MW:*

"Measuring space" explains how engineers at NASA's Jet Propulsion Laboratory perform tests on equipment designed for unmanned spacecraft. September 2005. **www.tmworld.com/2005_09**

"There's no place like space" details how engineers at General Dynamics C4 Systems develop and test communications systems for space missions. September 2004. **www.tmworld.com/2004_09**



Silicon DEBUG

DESIGN-FOR-DEBUG METHODOLOGIES AND DATA ANALYSIS CAN PAVE THE PATH TO GREATER EFFICIENCY IN CHIP VALIDATION IN TARGET SYSTEMS.

BART VERMEULEN, NXP SEMICONDUCTORS, AND
YU-CHIN HSU AND ROBERT RUIZ, NOVAS SOFTWARE

For reasons of cost, performance, power, and miniaturization, many electronic systems that once consisted of several printed circuit boards are now manufactured as a single semiconductor device. As a result of this complexity, previously accessible system signals can no longer be observed, and the process of isolating and analyzing silicon problems has become tedious and time consuming.

Using a process called silicon debug, engineers try to locate the sources of errors in their devices. They work to understand the root cause, correct or work around the root cause, and prepare the device so high-volume manufacturing can proceed.

Engineers currently use various software and hardware tools to debug silicon. But because failure modes are complex and often arise only in corner-case scenarios under at-speed operation of the system, external debug equipment is insufficient to track down the source of system failures.

Design-for-debug (DFD) methodologies offer a better solution. By embedding DFD logic right on a chip and then stimulating and evaluating it with commercial silicon debug and analysis tools, device manufacturers can make it possible for test engineers to view signals on a chip and track down the causes of failure.

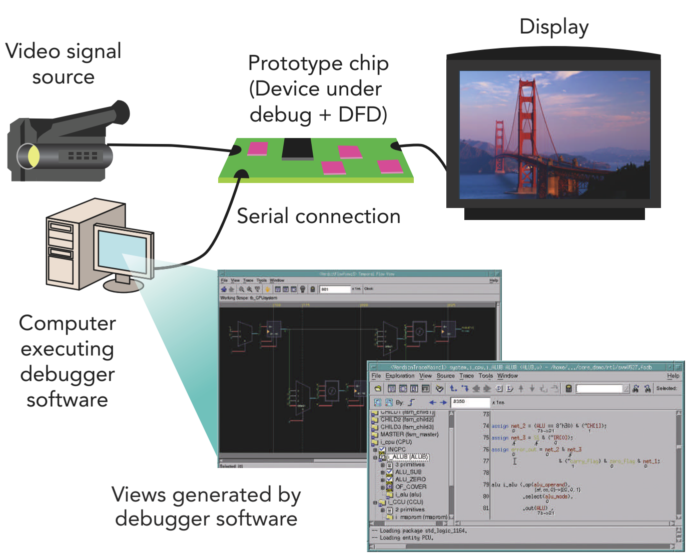
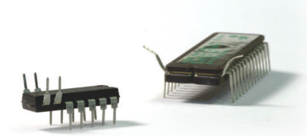


FIGURE 1. This application setup uses a debug architecture to obtain state data from a chip embedded in a system.

Using DFD logic

By adding DFD logic to chips, designers make it possible for test and product engineers to observe key internal signals and use a host-side commercial debugging tool to analyze and understand nonconformant chip behavior. One of the most popular silicon debug techniques is state dumping. This technique can be implemented using a standard on-chip DFD architecture that consists of only three debug features, which we call the "ABC" of silicon debug. An IEEE 1149.1 standard Test Access Port (TAP) controls all three features:

- *Access to the internal scan chains.* Reusing the internal scan chains, which are typically already inserted to facilitate chip manufacturing test, is a common way to enable easy debugging. Re-



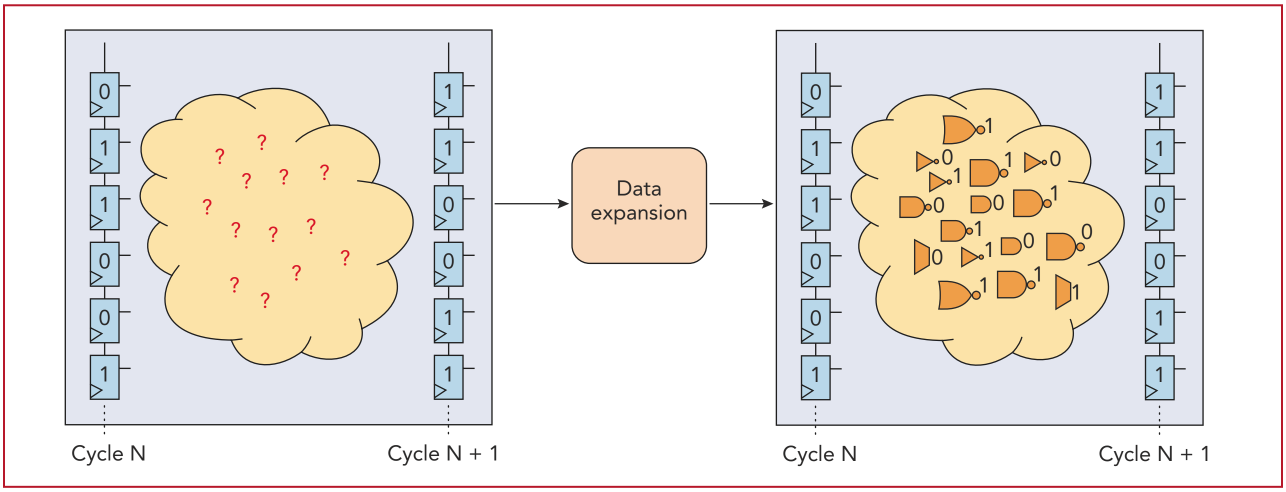


FIGURE 2. **As a result of data expansion in a debug environment, all computable combinational signals contain a Boolean value of 1 or 0.**

using the scan chains is inexpensive and provides the complete state of the chip when scanned out via the TAP.

- *Breakpoints.* When an important, internal event or sequence of events is detected, an on-chip breakpoint module stops the functional clock signals. This breakpoint is programmable via the TAP.
- *Clock control.* When the functional clock signals have been stopped, an on-chip switch is programmed to have the functional clock signals follow the TAP clock during scan out.

The resulting debug architecture scales well with the chip's number of clock domains and flip-flops, and we have found that its cost in terms of silicon area is typically well below 1% of the total chip area. The DFD logic provides full access to the internal signals at predefined points in time, while the chip is operating in its intended application board.

Figure 1 shows the setup we use to debug silicon. The setup uses the debug architecture to obtain state data from a chip embedded in a system. A desktop computer is connected to the on-chip TAP controller. Normal user-defined TAP instructions control this setup.

When using such a setup for your own debug application, your first step is to program the breakpoint, or the point in time when you want to take a snapshot of the circuit's state. Then, the chip is functionally reset and initialized in its environment to a known, stable state. The application starts to execute, and when the breakpoint is hit, the breakpoint is activated and the on-chip functional clocks stop.

The debugger software running on the desktop computer detects the stopped clock, switches the circuit into debug scan mode, and extracts the content of the on-chip scan chains. The resulting bit stream (referred to as a state dump) is stored on disk for further processing and interpretation. In most cases, this post-scan dump-data operation is performed by the debug system itself.

Your next step is to prepare the data for use with host-side debug systems. The software maps the data (which consists only of ones and zeroes) to its origin in the design and system time as follows:

1. For each scan data extraction, the software adds a time stamp or cycle number based on the breakpoint that was hit;
2. The software associates the data with the gate-level signal names in the HDL design; and
3. The software subsequently writes the data in a format such as the Value Change Dump (VCD) standard.

As an alternative to gate-level mapping, you can associate the data with signals at the register transfer level (RTL). Hardware designers trying to understand the behavior of their silicon often prefer this level of design abstraction.

Expanding the data

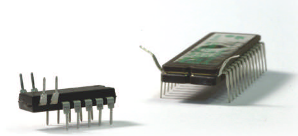
The scan dump is formatted into a VCD file. To allow you to observe internal signals not accessible via the DFD logic (for example, values are in the combinational logic clouds between the scan registers), the software computes the missing data through a process called "data expansion." In this process, the software

1. reads the mapped fan-in-cone scan register values corresponding to the internal signals to be observed;
2. sorts the combinational logic between these registers using a linear ordering algorithm;
3. computes the values for these signals using a cycle-based evaluation; and
4. creates a VCD file with the computed values.

(continued)

Table 1. Data expansion results

CASE	TOTAL SIGNALS	DUMPED SIGNALS	DUMPED-TO-TOTAL RATIO	EXPANDED SIGNALS	OBSERVED SIGNALS	OBSERVED SIGNAL PERCENTAGE
Circuit 1	347	110	32%	237	347	100%
Circuit 2	32,009	4,593	14%	25,560	30,153	94%
Circuit 3	138,842	13,190	9.5%	125,652	138,842	100%
Circuit 4	4,568,074	173,544	3.4%	4,356,475	4,530,019	96%



The result of data expansion is that all computable combinational signals contain a Boolean value of 1 or 0 (**Figure 2**). If some of the state values are not available (that is, are not provided in the scan dump), some circuit values cannot be computed. In the generated views, these values are denoted with the special value "NC" (not computed). The computed values from data expansion, along with the scan dump values, are passed to a debug system via the VCD file.

Expected data based on golden simulation results can help narrow down an error's root cause.

Although data expansion can be considered similar to simulation, it is not burdened with the computational overhead that a simulator requires for time processing. You could further optimize data expansion by dynamically generating the combinational signal values for display in a debug system rather than by using a VCD file.

Usually, software-based debug systems read VCD files dumped from pre-silicon design simulations to trace the root cause of errors detected prior to tape-out. Using VCD files containing information obtained from actual running silicon, and created using the steps described above, effectively makes the debug of silicon the same as for simulation.

Because most designers are familiar with their simulation-centric verification environment, they can now immediately assist with silicon debug. Designers can apply pre-silicon techniques to isolate the root cause of any problem, all while operating in their familiar tool environment. The standard capabilities available in debug tools include the ability to perform source tracing, waveform viewing, schematic viewing, and value annotation on any of the design views. If available, expected data based on golden simulation results can help narrow down an error's root cause by highlighting differences with actual silicon data.

Case studies

For a set of typical use cases, we measured the effectiveness of the data-expansion method. We selected modules of two real designs and dumped out all register values and input values of the designs. Then, we applied the data-expansion capability available in the Novas Siloti SilVE vis-

The future of DFD methodologies

The interest in using a structured and standard DFD methodology is growing as evidenced by the tripling in registration for the 2005 Silicon Debug and Diagnosis Workshop compared to that for the inaugural event in 2004. (The workshop is held in conjunction with the International Test Conference). In response to this interest, several vendors are developing commercial solutions that support emerging DFD methodologies. The reuse of existing DFT techniques such as scan chains and the TAP is a DFD methodology that can be readily adopted. With over half of all designs now outfitted with an IEEE 1149.1-based TAP, and more than 80% of designs containing scan chains, a DFD methodology reusing these test structures offers a viable option for most design teams.

We, therefore, foresee that cooperation between silicon manufacturers and electronic design automation (EDA) vendors will lead to industry-wide standardization in the area of silicon debug. This standardization will provide the catalyst for EDA vendors to develop tools that generate the DFD logic and automate its inclusion in a chip design. The industry also needs a standard format for sharing debug data among debugger tools, and the IEEE has begun such standardization activities through its P1687 and P1149.7 working groups.

Bart Vermeulen, Yu-Chin Hsu, and Robert Ruiz

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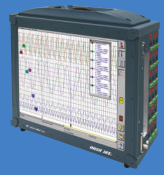

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ibility enhancement tool to calculate the missing values. **Table 1** shows the results.

While the size of the circuits varied significantly, the percentage of observable signals did not. The observable signals ranged from the mid-90s to 100% of all the signals. With this methodology, you can observe nearly all of the signals by dumping out only a limited number of registers and primary inputs for data expansion. This methodology also keeps the area impact to a minimum by leveraging already existing design-for-test (DFT) resources that would otherwise be idle during system-level debug.

Overall our approach bridges the traditionally separate environments of chip designers and silicon-validation engineers. The DFD logic can be readily used on all digital chips. The application allows engineers to share knowledge from both domains to find and resolve design errors in silicon more quickly and easily, yielding shorter time-to-market and higher product quality. T&MW

Bart Vermeulen *is senior scientist at NXP Semiconductors, founded by Philips. He has more than nine years of experience in SOC test and debug working for Philips Research, where he was involved in the definition and development of the debug strategy for a number of large Philips system chips. He has published more than 25 conference papers and holds two US patents on the topic of SOC debug. Vermeulen holds an MS degree from the Eindhoven University of Technology, the Netherlands.*

Yu-Chin Hsu, *VP of RD at Novas Software, is former head of the synthesis product line at Avant!. Hsu has over 16 years of R&D experience in EDA and has held faculty positions at the University of California and Tsing Hua University in Taiwan. Hsu holds a BS degree from Taiwan University and a MS degree and PhD from the University of Illinois.*

Robert Ruiz *is senior product marketing manager at Novas Software. Prior to joining Novas, he held various marketing and technical positions for the verification and test-automation product groups at Synopsys and Viewlogic Systems. He also has experience as an ASIC designer. Ruiz has a BSEE from Stanford University.*

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***Fluke 1897 & 189 Users Manual August 2000, Rev. 2, 6/02*

Agilent Technologies

TEST COMPRESSION

Does compression need to be 100 times better to support ever-increasing test-data volume and application time?

RON PRESS AND JAY JAHANGIRI, MENTOR GRAPHICS

Scan technology is essential for testing the digital content of large-volume devices. By using scan, you can make the device itself responsible for some of the "test" chores, and you can shorten the time needed for automatic test pattern generation. The key to setting up a successful scan-test operation is deciding exactly how much scan compression an application needs.

In scan-test mode, scan structures allow each sequential gate to be concatenated with other sequential gates and configured as a long shift register called a scan chain. Each sequential gate can be loaded with a predefined value and treated as a control point.

Once the device captures values into the sequential elements, an automated tester can enable scan test and "observe" results. Instead of trying to create patterns for a complex sequential circuit, all sequential gates behave as control and observe points. Overall, the test problem is reduced to testing the small blocks of combinational logic between the sequential gates. Scan simplifies the test problem enough that automated test pattern generation (ATPG) tools can quickly and efficiently create test patterns.

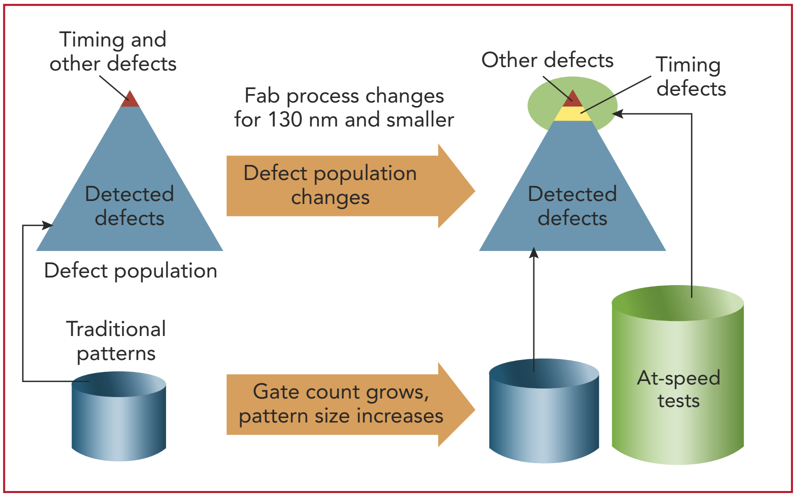


FIGURE 1. New tests related to timing are needed to cover new defects introduced by fab process changes.

Increases in test volume

Historically, as devices grew in gate count, scan test data volume and application time grew as well. A device that contains twice as many gates as the previous generation has scan chains that are twice as long, unless more scan chains are added. This is due not only to larger designs but also to the additional pattern types necessary to detect newer defect mechanisms. At the same time, these larger designs are moving to more modular and hierarchical design methodologies, creating the demand for fewer test signals from each circuit block.

As a result of the emergence of new fabrication technologies, standard stuck-at scan tests are no longer sufficient. Many companies have seen significant growth in the number of timing-related defects at 130 nm and below. At-speed scan testing has become necessary to detect this growing population of defects, but unfortunately, the most popular approach for at-speed scan requires a more complex pattern.

The most desirable application of at-speed scan test involves loading values into the scan chains at a slow clock rate and then applying two cycles at the system clock frequency. At-speed patterns can use internal PLLs for the at-speed launch and to capture pulses to provide accurate clocking. Because two cycles are required in the functional mode of these tests, at-speed scan patterns are typically three to five times larger than a stuck-at pattern set. Note that ATPG tools can support at-speed scan tests that are simpler and require fewer patterns—these are called launch-off-shift patterns. Such tools impose more design constraints, however, and will test more nonfunctional logic, possibly reducing yield.

In addition to using at-speed scan testing, some companies are starting to apply tests that target specific types of defects or the physical locations where certain defects are most likely to occur. One new pattern type statistically targets bridge defects that may have escaped stuck-at pattern tests. The idea is to detect a fault at each gate terminal multiple times while randomly changing how the fault is detected. This pattern type is referred to as multiple-detect pattern and can be created for stuck-at and transition faults.

Another new family of tests is based on targeting physical locations within the device layout database (GDSII) to identify the most likely defect locations. Since these tests use design-for-manufacturing (DFM) layout rules to identify the likely defect locations, they are often called DFM-based fault model tests. The first such fault model to be used is based on bridge extractions, and some manufacturers are using a combination of multiple-detect patterns and deterministic bridge extraction patterns (**Figure 1**).

As fabrication technologies evolve, test application time and test data volume are drastically increasing just to maintain test quality requirements (**Figure 2**). For example, new tests require:

- greater than 2X the test time to handle devices that double in gate count but maintain the same number of scan channels,
- 3X to 5X the number of patterns to support at-speed scan testing for the growing population of timing defects at 130-nm and smaller fabrication processes, and
- 5X the number of patterns to handle multiple-detect and new DFM-based fault models.

This equates to a minimum of 10X compression for increased design sizes and at-speed test patterns just to maintain quality and tester throughput. If newer multiple-detect or DFM-based fault models are added, then the test time will increase to 20X.

Thus, the starting point is 10X compression just to maintain tester throughput and 20X if new fault models are used, which becomes 40X if the next design doubles in size. If you consider reducing the block-level routing and top-level scan pins by 5X, that means you need 5X more compression on top of the existing compression. Supporting multisite testing or DFM-based fault models will triple the compression requirements at a minimum. A major benefit of compression is to reduce test pin count, which is a major cost benefit at manufacturing. As a result, some companies are already looking for compression well beyond 100X tester cycle reduction.

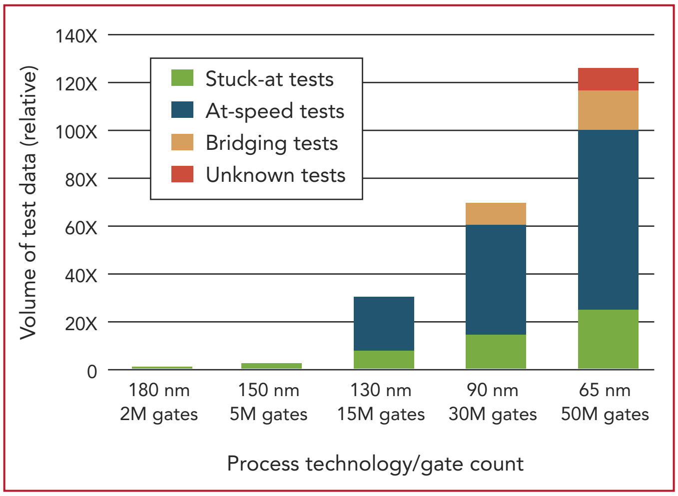


FIGURE 2. The number of tests and corresponding data volume increase with each new fabrication process technology.

Test-compression techniques

A few important factors to consider with any compression technique are:

- the amount of compression possible,
- the scalability of compression (does the compression technique work with various design sizes, with few or many scan channels, and with different types of designs?),
- the robustness in the presence of X states (can the design maintain compression while handling X states without losing coverage?), and
- the ability to perform diagnostics of failures when applying compressed patterns.

Popular scan techniques include Illinois Scan, a technique that involves connecting many internal scan chains to a common scan channel, and embedded deterministic test (EDT), which employs a combination of approaches to provide high compression while working in the presence of X states. The input side is called a continuous-flow ring generator (**Figure 3**). It is similar to a linear feedback shift register (LFSR) in that it can produce random data, but the device

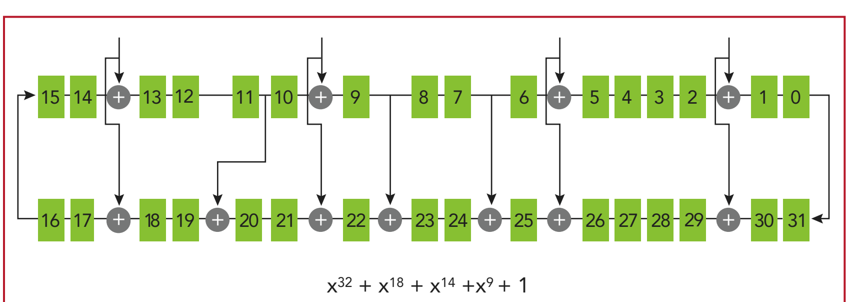


FIGURE 3. The embedded-deterministic-test decompressor shown here employs a continuous-flow ring generator.

is used to decode compressed data with every shift of scan channel values.

In Mentor Graphics' EDT implementation (see the sidebar "Modular embedded deterministic test" accompanying the online version of this article at www.tmworld.com/2006_10), the initial ATPG process of determining which values to load into scan cells to detect as many faults as possible is exactly the same as in standard ATPG. This is true for any type of scan pattern. But if standard ATPG were used, it would use random values to fill up the unspecified scan cells that cannot improve targeted fault detection.

Instead, EDT processes the desired specified bits for the pattern and determines how to load them through the decompressor. When the resulting compressed pattern is loaded through the decompressor, the specified bits get loaded into their respective scan cells. A side effect of the decompressor is that all the unspecified bits get loaded with random data. As a result, lots of tester cycles are saved by not having to specifically load random data.

In a tester using EDT, scan-chain outputs feed into a compactor. Several scan chains are XOR-combined into individual scan channels. Each scan chain only propagates to one gate with this configuration, which controls routing congestion.

One of our most important considerations when developing the EDT architecture was how to handle X states. Even if no X's are present in the design, the design may still need to accommodate X's when considering false and multicycle paths for at-speed patterns. Otherwise, there could be huge losses in test coverage and compression.

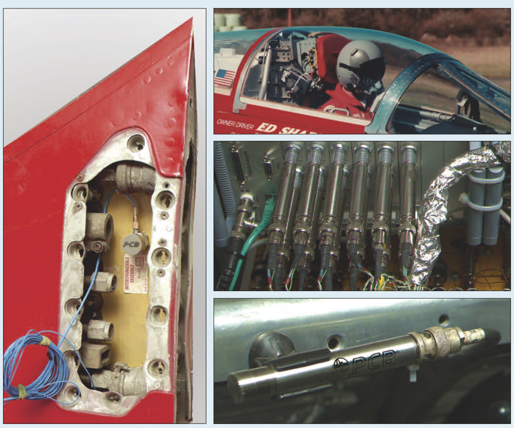
The EDT compactor has a masking capability at each scan chain output (**Figure 4**). Masking is only used when a fault that was specifically targeted is disrupted by an X propagating to the same scan channel. EDT determines when masking is needed automatically during pattern generation. Values are loaded into the mask register during scan chain loading so no special tester protocol is needed. The decompressor treats the values as specified bits that are automatically solved during pattern generation.

In EDT, many internal scan chains are loaded through a small interface of several scan channels. The ratio of internal scan chain to channels defines the maximum possible compression. EDT provides the following capabilities:

- very high levels of compression—many devices have been designed with effective compression in the 100X range;
- scalability—effective compression is possible with just one scan channel and

Table 1. Illinois vs. EDT scan effectiveness

DESIGN	GATES	METHOD	COVERAGE	VOLUME	COMPRESSION
A	543k	ATPG	98.83%	61M	1.0
		Illinois	97.45%	2.8M	21.9
		EDT	98.85%	1.3M	46.8
B	576k	ATPG	98.71%	75M	1.0
		Illinois	98.48%	2.1M	35.5
		EDT	98.71%	1.3M	57.0
C	1.2M	ATPG	97.06%	578M	1.0
		Illinois	96.75%	10M	57.3
		EDT	96.99%	7.7M	75.6
D	1.2M	ATPG	99.88%	25M	1.0
		Illinois	95.16%	2.7M	9.2
		EDT	99.86%	0.8M	32.1
E	1.5M	ATPG	99.04%	59M	1.0
		Illinois	98.17%	2.8M	21.5
		EDT	99.03%	1.6M	38.1
F	2.1M	ATPG	98.86%	193M	1.0
		Illinois	96.95%	11.7M	16.5
		EDT	98.84%	4.3M	44.8



has been used in smart cards that have only a three-pin test interface;

- compressed pattern diagnostics;
- no loss of coverage in the presence of X states, making possible the masking capability; and
- flexibility—the EDT logic is only based on the number of scan chains and works as a transform function (with no need to change the EDT logic due to core design changes as long as the number and interface to scan chains remains constant).

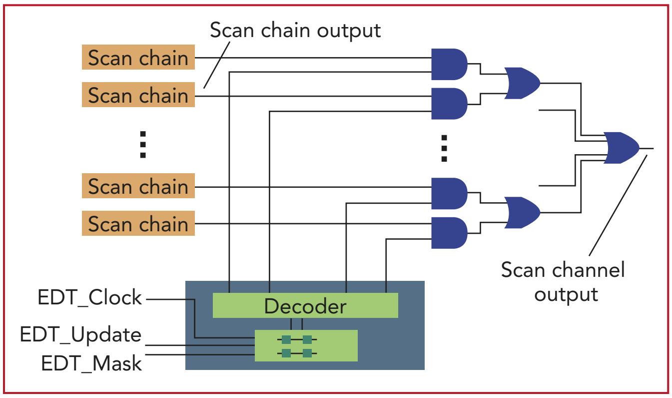


FIGURE 4. An EDT compactor can mask unknown states from disrupting fault detection.

To demonstrate the compression value of EDT technology, we evaluated six designs using both ATPG without compression, EDT, and Illinois Scan (**Table 1**) with the same scan-chain-to-channel ratio on the input side. For accurate comparison, no compaction was used on the output.

We found that the highest coverage using standard ATPG was reached by EDT for all six designs. Also, the EDT compression ratio (normalized for the coverage achievable by Illinois Scan) is noticeably better. As a result, a design configured with EDT compression logic can accommodate more patterns of various types within the same tester data volume and test application time. Even greater compression can be achieved by using the EDT compactor on the output that is capable of masking unknown states. Using a compaction technology without masking can result in huge coverage loss and lower compression. T&MW

Ron Press *received a BSEE from the University of Massachusetts and has worked in the test and built-in test industry for more than a decade. He is the technical marketing manager for the Mentor Graphics design-for-test division in Wilsonville, OR.*

Jay Jahangiri *is a technical marketing engineer for Mentor Graphics' design-for-test products. He worked as a DFT engineer for Texas Instruments and Raytheon before joining Mentor Graphics in 2000. He has a BSEE and an MBA.*

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Vote for the 2007 TEST ENGINEER *of the Year*

Our editors selected six finalists for this annual award. To help choose the winner, cast your ballot by November 3.

Testing is the cornerstone of successful development and manufacturing for any electronic component, system, or end product. Without testing, quality is just a dream. The test engineer builds in quality—from design to production—and often plays a critical role in identifying in-service issues or introducing product improvements.

To recognize the vital role that the test engineer plays and to salute the creativity and hard work that goes into making products safer, more reliable, and more economically viable, *Test & Measurement World* announces its fourth annual Test Engineer of the Year competition. Thanks to the generosity of the award sponsors—Agilent Technologies, Keithley Instruments, and National Instruments—the winning candidate will designate a $30,000 donation to an engineering school.

From the many engineers who have been nominated for this award over the past few months, our editors have selected six individuals as the finalists, which we first announced in our September issue. There's still time for you to cast your vote (using our online ballot) before the November 3 deadline. When reviewing the summaries of the finalists' accomplishments, please consider both their on-the-job skills as well as their overall contributions to the test field and the industries they serve.

Test & Measurement World will present the 2007 Test Engineer of the Year award at our "Best in Test" gala during the 2007 APEX Show (February 20–22, 2007, Los Angeles Convention Center). In addition, the cover story of our March 2007 issue will profile the winning engineer.

THERE'S STILL TIME TO VOTE!

DEADLINE: NOVEMBER 3, 2006

WWW.TMWORLD.COM/TEOTY

AEROSPACE

Pavan Bathla

Moog

As test equipment lead for the remote electronic units (REUs) at Moog, a manufacturer of control products for the aerospace industry, Pavan Bathla is responsible for estimating the time, cost, level of automation, resources, and skill sets required for testing. He chooses the tools and platform, architects the hardware and software, and breaks down the tasks for his team to perform.

Due to the production volumes on the REU, Bathla chose what he calls an asynchronous concurrent and reject test strategy, which tests the different REU types in parallel and halts tests on initial failure detection. This strategy provides the highest possible throughput and device utilization, thereby saving his company time and money. He demonstrated expertise in the architecture of the ATE by getting the Simulink actuator model, more than 400 switch permutations, and data-acquisition hardware on both the Windows and PXI-real-time operating systems to all work together in harmony. By using a PXI platform rather than the proprietary DSpace system the company traditionally used, Bathla significantly reduced the cost of hardware-in-the-loop simulation.

In addition, he has led the test software philosophy team for his division and has spearheaded user group meetings. Bathla maintains a blog called Synergy Energy, which is his channel for sharing knowledge and collaborating with counterparts in the industry.

METROLOGY

Jay L. Bucher

Promega

Currently manager, metrology services, at Promega, a maker of products that help researchers in the life sciences, Jay Bucher boasts a lengthy career in testing—including 24 years working in US Air Force calibration laboratories. Many of Bucher's efforts have benefited the worldwide metrological community. For example, he helped create the American Society for Quality (ASQ) Certified Calibration Technician (CCT) Program and is a subject matter expert for exam questions.

Bucher is editor and co-author of *The Metrology Handbook* and *A Quality Calibration System: Developing and Managing a Calibration Program*, both issued by ASQ Quality Press. He is also the managing editor and publisher for the ASQ metrology-focused quarterly publication, *The Standard*, and he has published several papers and made a number of presentations to professional groups.

Over the years, Bucher has served as a division officer for ASQ Measurement Quality Division (MQD) in several capacities and currently is MQD treasurer. He has organized and coordinated a new section in Wisconsin for the National Conference of Standards Laboratories International (NCSLI) and currently is the North Central Regional Coordinator for NCSLI. Bucher is a recipient of the Max J. Unis award, which honors outstanding contributions to the metrological community and is the highest recognition available from ASQ MQD, and he also received the NCSLI 2005 Region/Section Coordinator of the Year Award.

RF TEST

Stephen J. Cousineau

Skyworks Solutions

Stephen Cousineau is RF production test development manager at Skyworks Solutions, a maker of radio solutions and precision analog semiconductors. He works exclusively in the production test environment, where even a few milliseconds of test time savings is important.

While the ATE systems at the company were able to perform parallel RF testing and the test handlers could perform multisite testing, these capabilities were not being used because of two technical road blocks. First, the tester did not have sufficient RF resources to address all of the I/O ports on a cellular phone transmitter (TX) front-end module in a multisite mode. Second, because the load board was of hard-dock design, it was impossible for engineers to create a load-board layout that did not compromise one of the sites for RF measurements.

Cousineau found the key was expanding the capability of the RF test head through the use of an internally designed RF multiplexer containing switching, filtering, coupling, and amplification. The new RF multiplexer is housed in a fixture that mounts to the test head and soft docks (with flexible RF cables) to the test handler. Custom test code calibrates and controls the RF multiplexer. With this new system, test time has been cut in half and throughput has been doubled.

ENVIRONMENTAL TEST

Clayton Forbes

National Technical Systems

Clayton Forbes is the senior dynamics engineer for NTS, an engineering and testing services provider. As the program manager on a qualification and acceptance test program for engine hose assemblies manufactured by Smiths Aerospace for the Space Shuttle, Forbes worked closely with Smiths Aerospace, Boeing, and the United Space Alliance to enable a tight deadline to be met on leak, flow, pressure, and burst testing. When the USS Nimitz aircraft carrier required vibration testing on an onboard file server for the storage of aircraft technical data, Forbes answered the challenge, designing a test fixture to accommodate the 7.5x6x3.5-ft, 3770-lb file server.

In addition to his lab work, Forbes supports customers in aerospace, defense, transportation, electronics, and telecommunications, in both the US and Europe, providing training and consulting services on product design for compliance and reliability. He takes an active role in the development of standards as a participant in the GR-63-CORE Issue 3 and MIL-STD-810G working groups and in the ANSI T1.E1 committee developing compliance standards for telecommunications equipment. Internally, Forbes provides training in dynamics theory and test troubleshooting, enabling best practices to be deployed across the NTS network.

COMMUNICATIONS TEST

John Gmitter

Harris

John Gmitter is a lead test engineer in Harris Corp.'s RF Communications Division, which designs and manufactures secure radio systems. Gmitter and his team needed to create a "next generation" test platform that would consume less floor space, reduce test times, cost less, and be expandable for increasing throughput.

In particular, the engineers needed to move away from a set of test instruments that was no longer going to be supported by the manufacturer. Gmitter and his team evaluated multiple platforms and hundreds of instruments and ended up developing a modular hardware platform and software architecture that allowed instruments to be interchanged. The architecture supports parallel testing and high instrument utilization. The system, which is built from off-the-shelf hardware and software, can incorporate additional instruments when required. The project accomplished all of the stated goals and is expected to give Harris a competitive advantage.

SEMICONDUCTOR TEST

Eric R. Ramelli

Philips Semiconductors

A senior test engineer at Philips Semiconductors, Eric Ramelli has a strong knowledge of the Credence Vista series and the Agilent 93K testers, and he has become a valued mentor for other engineers. He has also helped solve problems when the company has encountered tester limitations. In one case, Ramelli created binning on the ATE to help the production facility pinpoint tester issues. One product being tested required a resistive measurement of 10 Ω. Such small values are difficult to measure due to factors such as tester driver resistance, socket resistance, and contact resistance.

Once an accurate measurement procedure was developed, Ramelli needed to help the production facility determine when the tester hardware was generating incorrect measurements that were causing good parts to fail, such as when a dirty socket added contact resistance. These complications needed to be caught quickly to prevent the rejection and disposal of good parts. Ramelli helped devise many methods—such as a delta resistance calculation between pins—that enabled the test floor to pinpoint troubles. He also developed a test program to allow a microcontroller to trim out its internal RC oscillator circuit. Older methods had extreme test time, which consumed resources. The new test method allows a square wave to be used for comparison purposes to generate the value to be used in the program. T&MW

Digitizers offer three channel counts

For digitizing applications that require high-speed sampling and data streaming, you can use the UF2-3130 series of digitizer cards from Strategic Test. The

12-bit, 25-Msamples/s cards come with two, four, or eight channels. They use a 66-MHz PCI-X bus to stream data at 225 Mbytes/s to the standard 64 Mbytes of memory (4 Gbytes are optional).

The cards let you adjust sample rate so you can maximize memory use when you don't need to sample at full speed. Each channel has its own amplifier and ADC, which means you can sample all channels simultaneously. The UF2-3130 series features options such as gated triggering and four TTL digital inputs per analog input. Thus, you can read digital status signals synchronously with analog measurements.

Software support includes drivers for Windows and Linux. Optional drivers for Matlab, LabView, Vee, Dasylab and LabWindows/CVI are also available.

Prices: two channels—$4690; four channels—$6190; eight channels—$10,390. *Strategic Test, www.strategic-test.com.*

Aeroflex adds software update to 2975 test set

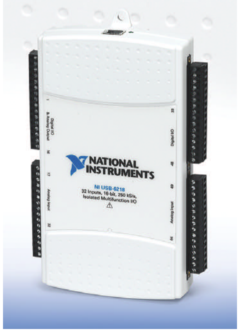
Aeroflex has announced a new software version—Release 1.9.2—for its 2975 Project 25 radio test set. The new software adds eye-diagram functionality for P25 waveform analysis. With this diagram, users can quickly see the C4FM (compatible four-level frequency modulation) deviation points as well as any offset or imbalance in the four frequency levels corresponding to C4FM modulation (±600 Hz and ±1800 Hz). This new eye diagram feature is included in Option 2975OPT30 Modulation Analysis and is free of charge.

In addition, Release 1.9.2 has a new configuration to simplify the ordering of LSM testing options. Options 11 (LSM/Phase 2) and 13 (LSM Advanced/P25 Phase 2 Advanced) have now been combined into a single option—the 2975OPT29 CQPSK (compatible quadrature phase shift keying) Generate/Receive and Analysis option, which provides tests for linear simulcast modulation.

The 2975 is a digital radio test platform that tests radio equipment to ensure proper operation to various Project 25 standards (www.p25.com), including parametric testing for compatible four-level frequency modulation and interoperability testing of P25 systems.

Base prices: 2975—$21,495; Release 1.9.2—free; 2975OPT30 Modulation Analysis option—free; 2975OPT29 CQPSK Generate/Receive and Analysis option—$8000. *Aeroflex, www.aeroflex.com.*

USB data-acquisition modules take power from bus



National Instruments has expanded its USB line of data-acquisition modules by introducing four bus-powered modules that feature the performance of the company's M series instruments. The new USB-621x series also increases sampling rate for the company's bus-powered USB modules from 50 ksamples/s to 250 ksamples/s with 16-bit resolution. All models in the series include two 32-bit counter-timers for frequency measurements, timing, and totalizing. The USB-6215 and USB-6218 have analog inputs with 60-V isolation.

MODEL	ANALOG INPUTS	DIGITAL IN/OUT	ANALOG OUTPUTS	PRICE
USB-6210	16	4/4	none	$499
USB-6211	16	4/4	2	$699
USB-6215	16	4/4	2	$899
USB-6218	32	8/8	2	$1099

National Instruments, www.ni.com/usb.

Genesys 2006.07 addresses ease of use

Agilent Technologies has updated its Eagleware product line with the release of Genesys 2006.07, a new version of the company's RF and microwave design software. The enhanced optimization in Genesys 2006.07 includes improved modeling for faster solution convergence.

The new release supports eye diagrams to help with the analysis of complex RF modulated signals and to

> > > > > > >

help determine the effects of digital-signal interference. New examples and learning tools are also included, such as tutorials to help with creating datasets, with scripting, and with equation writing.

Base price: $5000. *Agilent Technologies, www.agilent.com/find/eesof.*

SONET/SDH modules

Exfo has added optical transport network (OTN) testing to its IQS/FTB-8120 and IQS/FTB-8130 Transport Blazer SONET/SDH test modules. The IQS/FTB-8120 (2.5 Gbps) and IQS/FTB-8130 (10 Gbps) combine SONET/SDH, next-generation SONET/SDH, and now OTN testing, as defined in ITU-T G.709, in a common platform to help streamline customers' testing needs.

The OTN software option runs on the IQS-500 test system for manufacturing and R&D test applications. It can also be used with the FTB-200 compact platform and the FTB-400 universal test system to ensure coverage of a wide array of test and measurement applications, ranging from R&D verification to field turn-up and troubleshooting. It includes forward error correction (FEC) generation and analysis, as well as support for all OTN layer alarms and errors. The OTN software supports both OTU1 (2.7 Gbps) and OTU2 (10.7 Gpbs) test rates.

Exfo Electro-Optical Engineering, www.exfo.com.

Vector signal generator

The p1411A RF vector signal generator from PrecisionWave features a spectrum-analyzer display along with an internal IQ waveform generator. The instrument is available in benchtop or ATE configurations. Serving the 800-MHz and 1700-MHz cellular bands, the p1411A produces EDGE, GSM, IS-95, NADC, PHS, WCDMA, and CW signals. User-created IQ waveforms can generate other signal types, specify data content, or create worst-case signal scenarios for development and test of RFICs, subassemblies, or completed wireless products.

PrecisionWave's spectrum analyzer display continuously shows the instrument's output without necessitating the use of an expensive external spectrum analyzer. A 7-in. TFT display includes a touch panel for easy instrument control without external mouse, stylus, or keyboard, though these may be connected. The instrument supports LAN programming of automated R&D or manufacturing applications within the Microsoft

Visual Studio or Microsoft Visual Studio .NET environments. The instrument may also be controlled and monitored from Web applications.

Base price: $9990. *PrecisionWave, www.precisionwave.com.*

Time and frequency receivers

Symmetricom now offers its XLi and XLi SAASM Series of GPS synchronized time and frequency receivers with an HTML Web interface that improves the net-centricity of the in-

struments by providing a remote graphical user interface. The Web interface, which will come standard with all units, simplifies access to status, configuration, control, and support of the product.

The company is also offering Windows-based time monitor software that performs automatic collection of time and frequency measurements, as well as a wide range of time and frequency computations, including frequency offset, drift, stability (Allan Variance), MTIE/TDEV wander, phase deviation, and more. In addition, the time monitor software allows easy plotting of data with a choice of five different graph types and supports numerous telecom masks (ITU-T, ANSI, ETSI), which can be overlaid on the plot.

Symmetricom, www.symmetricom.com.

RF reference source

Fluke has released the 9640A RF reference source that covers 10 Hz to 4 GHz with a best level accuracy of ±0.05 dB. The source combines level precision, dynamic range, and frequency span in a single unit in order to calibrate a wide range of RF test equipment.

Fluke's MET/CAL automatic calibration-measurement software supports the source with a range of common RF workload procedures. The source outputs a pure sinewave to eliminate differences between wide- and narrow-band or peak and rms sensors without external filters. The leveling head maintains precision and noise immunity over a –130-dBm to +24-dBm range. The standard head has 50-Ω characteristic impedance with 75-Ω as an option.

Fluke, www.fluke.com.

Serialization support

BPM Microsystems has announced it has added support for device serialization using FX4 and FX2 socket modules. This serialization feature was integrated with the release of BPWin 4.62 to accommodate what the company calls the increased demand for enhanced 7th generation device-programming technology. Previous versions of software allowed for device serialization using only single-socket modules.

All algorithms added to future BPWin software releases will support this new feature, although customers seeking FX4 and FX2 device-serialization support for algorithms released prior to BPWin 4.62 will need to enter a device request through BPM's Web site. All 7th generation customers with a current software support contract can download the latest software version.

BPM Microsystems, www.bpmmicro.com.

Stereo vision system

Designed as a drop-in replacement for its predecessor, the Bumblebee2 stereo vision camera system from Point Grey Research acquires 48 frames/s at a resolution of 640x480 pixels (VGA) or 18 frames/s at a resolution of 1024x768 pixels (XVGA), depending on the model. Both models come in color and monochrome versions with a choice of 3.8-mm or 6.0-mm focal length lenses.

The binocular Bumblebee2 employs two ⅓-in. progressive-scan CCD sensors and transmits both the left and right images to a PC via an IEEE 1394 interface. The system is precalibrated for lens distortions, and the left and right images are aligned within 0.05-pixel rms error. Calibration files are embedded in the camera allowing the supplied software to retrieve the image correction information.

The included Digiclops and Triclops software development kits enable you to control camera settings, adjust image quality, and access real-time depth range images. Sample programs and source code are also included.

Point Grey Research, www.ptgrey.com.

Waveform viewer

The new M1 Waveform Viewer from Amherst Systems lets you capture data with different oscilloscopes and save it in a common format for plotting and analysis. The software makes it easy to share your data with colleagues or customers who use a different scope.

Using the M1 Waveform Viewer, you can capture data from scopes made by Agilent Technologies, LeCroy, Tektronix, and Yokogawa. You can save the data in comma-separated variable (CVS), Microsoft Excel (XLS), or Agilent BIN format, and you can analyze the data without importing it into Excel or other pro-

grams. Analysis features include automatic pulse-parameter measurements, multi-acquisition analysis, multi-acquisition statistics, Lock-X-axis, and global markers.

The software's data-source window lets you navigate and analyze multiple waveforms simultaneously from different sources. Its user interface is a simplified enhancement to the company's M1 Oscilloscope Tools. Thus, you can use a common user interface regardless of oscilloscope.

Price: The M1 Waveform Viewer was initially offered as a free download, but the company reserves the right to charge for downloads without notice. List price is $145. *Amherst Systems, www.Amherst-Systems.com/M1_WV.html.*

Insulation testers

Megger's family of eight insulation testers offers test voltages from 10 V to 1000 V for installation, maintenance, service, and repair work in the electrical, power, and telecommunications industries. Each instrument features dual digital and analog arc displays that simultaneously show both the measurement result and the actual test voltage being delivered.

To meet low-voltage insulation testing requirements, the instruments deliver test voltages from 10 V to 100 V selectable in 1-V increments. They also include an insulation resistance measurement range that extends from 20 GΩ to 200 GΩ, with the option to display the insulation test voltage or leakage current on the secondary display.

Measurement of cable distance by capacitance is included on two of the models, providing a convenient cable length test. Some models also furnish timed insulation tests for polarization index and dielectric absorption ratio measurements. A 200-mA continuity measurement is available with 0.01-Ω resolution for fast, accurate cable resistance measurements. All units conform to IEC1010-2 for Category IV 600-V applications.

Megger, www.megger.com.

Ready-to-run DAQ software

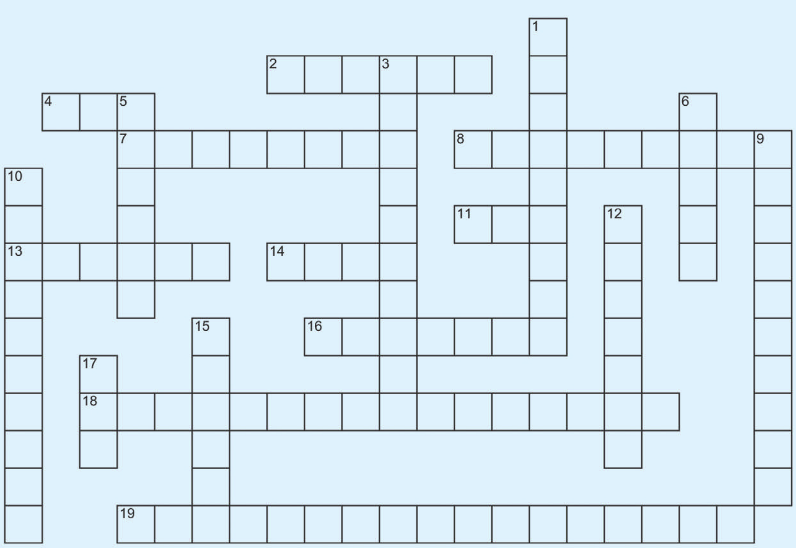
A new software application from Data Translation can help you acquire data from the company's USB or PCI data-acquisition products. With the .NET-compatible quickDAQ, you can acquire and plot data in real time at acquisition rates up to 2 Msamples/s.

The software lets you specify input channels and how to display data

Instrument Interlude

ACROSS

- **2** Detector, kind of
- **4** Common Spectral Analysis Algorithm (acronym)
- **7** Sine, square, triangle, and sawtooth are examples
- **8** Run until structure for continous execution
- **11** PCI Extensions for Instrumentation
- **13** Make or break an electric circuit
- **14** Programmable logic hardware (acronym)
- **16** External stimulus that initiates instrument functions
- **18** Software used to easily connect to instruments
- **19** LabVIEW-based function



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DOWN

- **1** PC-Based Oscilloscope
- **3** Software emulation of certain behaviors
- **5** Number of years since LabVIEW invention
- **6** Unwanted signals
- **9** Next generation, high-bandwidth, high speed PC bus based on PCI
- **10** Instrument that measures the viscosity of transparent liquids and gases
- **12** Revolutionary graphical development software for test, control, and design applications
- **15** Deviation from an ideal timing event often seen in clocks
- **17** Most commonly used control algorithm (acronym)

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using numerical, graphical, or gauge readouts. You can view data in real time or store it for analysis later. You can also export data from quickDAQ into other applications such as Excel or Matlab for analysis.

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Price: $195. *Data Translation, www.datatranslation.com.*

Fax test tool

FaxLab 6, the latest upgrade of QualityLogic's fax interoperability test tool, adds 12 V.34 profiles and 12 V.17 profiles for emulating multifunction peripherals from a variety of manufacturers at various resolutions and compressions. With this release,

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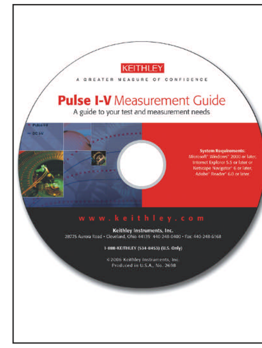

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QualityLogic, www.qualitylogic.com.

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Promation has introduced three new versions of equipment for sorting and rework after automated optical inspection is performed. To meet the needs of a variety of manufacturing processes, this new series has been designed to provide in-line sorting in configurations that meet each manufacturer's inspection and sorting requirements.

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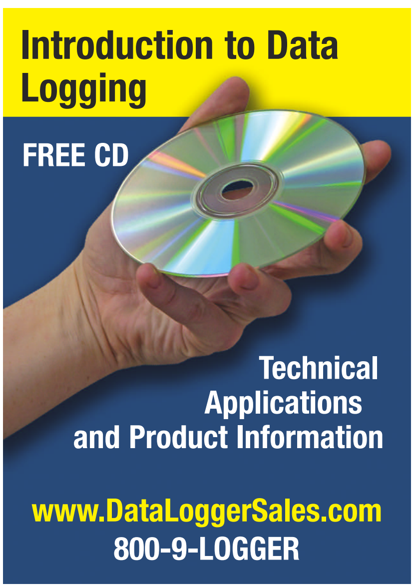
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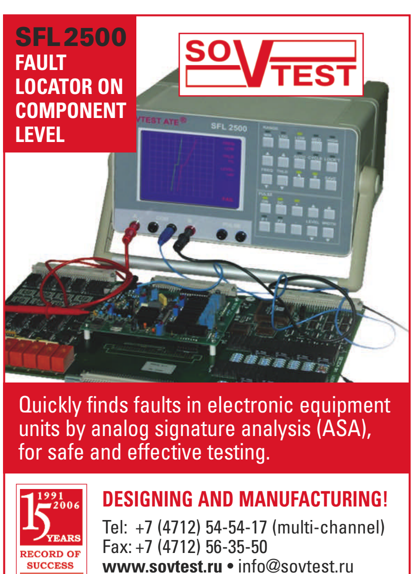
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BRUCE HOFER
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Bruce Hofer cofounded Audio Precision in 1984 with a group of audio engineers from the labs of Tektronix. In addition to serving as board chair, Hofer remains technically active as the company's principal analog design engineer. He has received 12 patents and has published many articles and papers, and in 1995 he received the Fellowship Award from the International Audio Engineering Society (AES). Hofer earned his BSEE degree from Oregon State University in 1970.

Contributing editor Larry Maloney spoke with Hofer about trends in the audio test market in a recent telephone interview.

How test answers the audio boom

Q: This year, your company surveyed engineers on the "future of audio." What did you find?

A: Probably the most significant finding was confirmation of an emerging multichannel market that we've been sensing for years. The survey showed that the percentage of engineers needing audio analyzers with only two channels is expected to drop from 62% today to about 37% five years from now. For the same period, the percentage of those who require six channels or more is expected to rise from 16% to 33%.

Q: What are the biggest changes in audio, and how are they affecting test?

A: Over the last decade, we've seen a progressive increase in digital content in audio products, and I don't mean just analog-to-digital converters. Signal processing has moved almost entirely from the realm of analog design to digital. Among the benefits are greater versatility and accuracy, and the implementation of audio features that were impractical with analog, such as very sharp bends, limiting filters, and artificial reverberation.

But there's a dark side, too, in that the audio contains digital artifacts that we call out-of-band noise. This energy is well above the audio band, and while it will never get to your loudspeaker, it can have some very interesting effects on the next device that you hook it to, as well as to your test instruments. We need to use very sharp bandwidth-limiting filters to exclude the effects of this out-of-band noise.

Q: How about the evolution in audio products?

A: Audio devices deliver an increasing level of functionality, often in very compact packages. We're witnessing a fusion of what were once distinctive or classic products, such as the cell phone. Now, the cell phone is being merged with a digital camera, and how long will it be before we see the cell phone merged with an MP3 player? Audio products are growing more sophisticated, more multipurpose, and more portable. All this influences the features that engineers will want to test. At the same time, we see high-end, multichannel audio systems for home theater and for automotive. It's not uncommon for cars to have 10-, 12-, or even 14-channel systems.

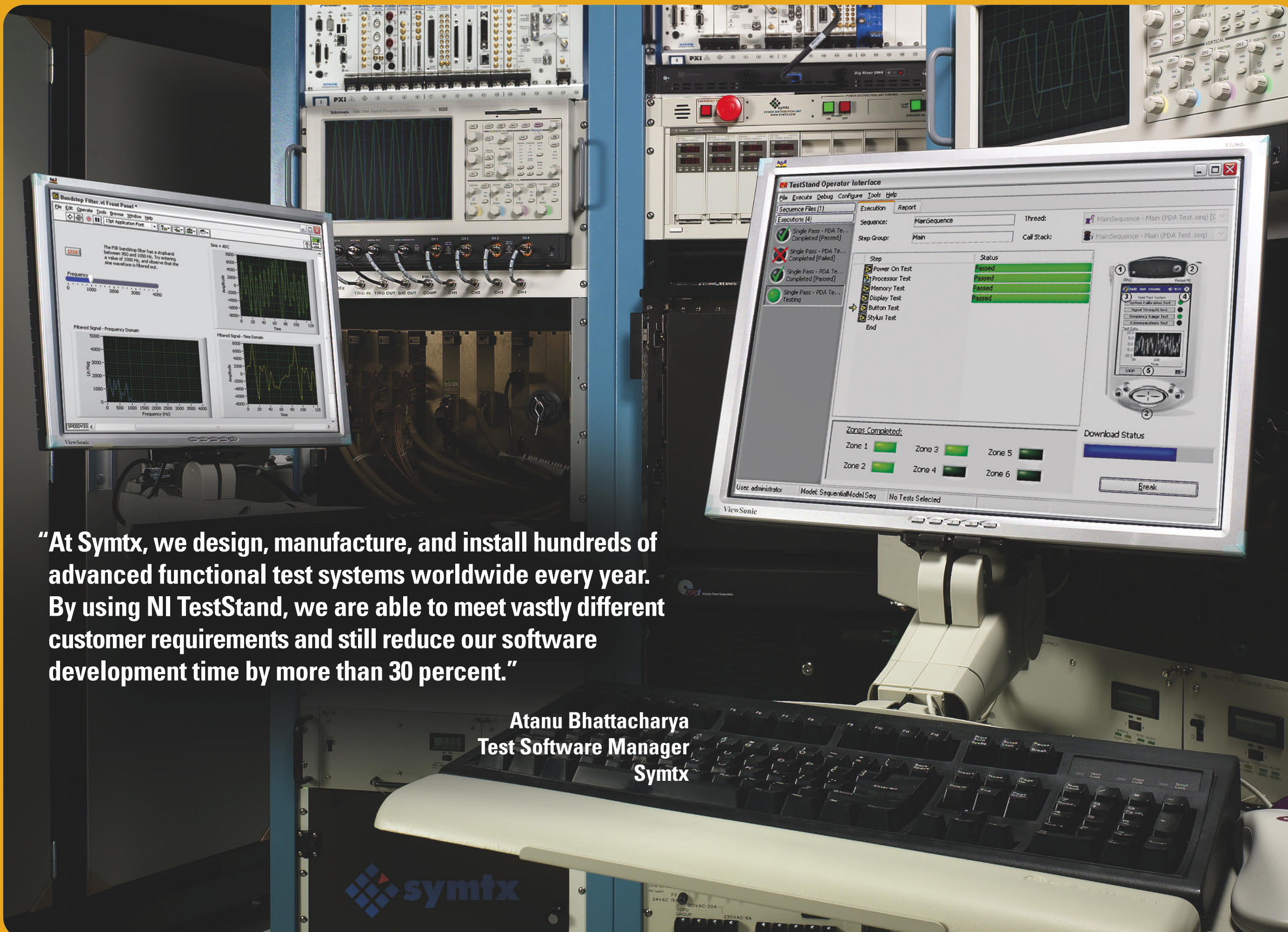
Q: How are these developments affecting your instrument offerings?

A: To address this growing multichannel market—from autos to Dolby 7.1 to traditional mixing consoles—we introduced our APx585. This analyzer, which comes with easy-to-use PC-based software, features eight analog audio inputs and eight analog outputs. It also supports eight channels of digitized audio. This ability to test more than two channels at any one time has obvious throughput benefits for test engineers and their companies.

Q: Do you see a greater need to serve engineers who don't have a strong audio background?

A: A very strong "yes." Many technical schools are focusing more and more on digital technology, and less on analog. Many R&D facilities also are designing consumer products that need to be mass-produced, typically offshore, by contract manufacturers. In those locales—China, Southeast Asia, and so forth—you find a wide variety of backgrounds in production test engineers. Many of them have not been exposed to some of the specialized parameters that we measure in audio, such as distortion or signal-to-noise ratio. So, a growing part of our job is providing the training and support that these engineers need. T&MW

Bruce Hofer comments on ease-of-use challenges, audio products, new application support programs, and other issues in the online version of this interview: www.tmworld.com/2006_10.



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